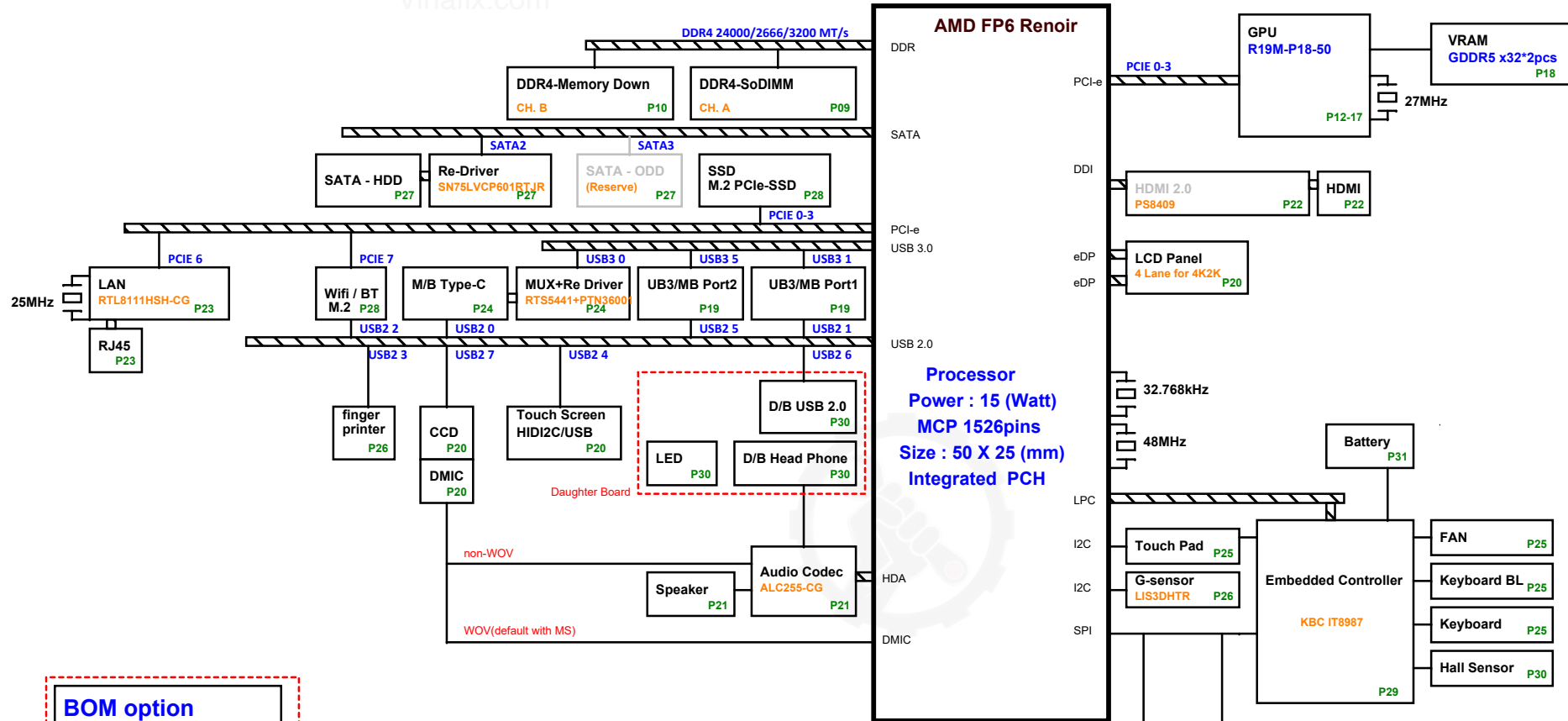


# ZAUR AMD Renoir Platform Block Diagram

01

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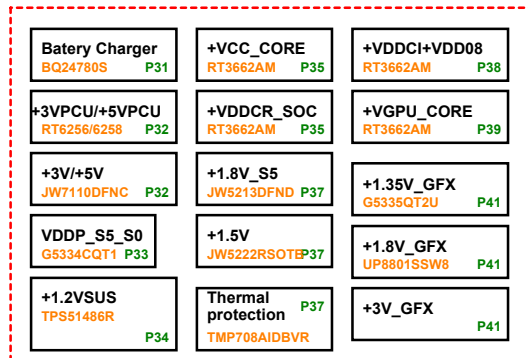


## BOM option

IV@ : UMA  
EV@ : DIS  
TPC@ : Type-C function  
TPC\_N@ : No Type-C function  
TSI@ : Touch screen HIDI2C  
TSI\_N@ : no Touch screen HIDI2C  
TPM@ : Trusted Platform Module  
TPM\_N@ : no TPM  
PBA@ : Finger Print on touch pad  
KBL@ : Keyboard back light  
GS@ : G-Sensor function  
GS\_N@ : No G-Sensor function  
SSD@ : Solid State Disk  
ODD@ : Optical Disc Drive  
RAM@ : On Board Memory  
DBG@ : for Debug Card  
255@ : Codec 255  
256@ : Codec 256  
FOR15\_17@ : Panel 15 or 17 inch  
\*FOR14@ : Panel 14 inch  
HDT@ : AMD HDT  
MID@ : Memory ID  
\*MS@ : Modern standby

G2@ for WW  
G3@ for MGF  
G3S@ MGF wo HDD connector

## Power solution



## PCB 8L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : SVCC  
LAYER 5 : IN2  
LAYER 6 : IN3  
LAYER 7 : SGND  
LAYER 8 : BOT

AMD APU	TOP BSQ	QBCON

PCIe Port	Function
PCIe_0	SSD_PCIe
PCIe_1	SSD_PCIe
PCIe_2	SSD_PCIe
PCIe_3	SSD_PCIe
PCIe_4	NA
PCIe_5	NA
PCIe_6	LAN
PCIe_7	WLAN

SATA Port	Function
SATA_1	M.2_SSD
SATA_2	HDD
SATA_3	ODD



PCIe-SSD be 4 lane

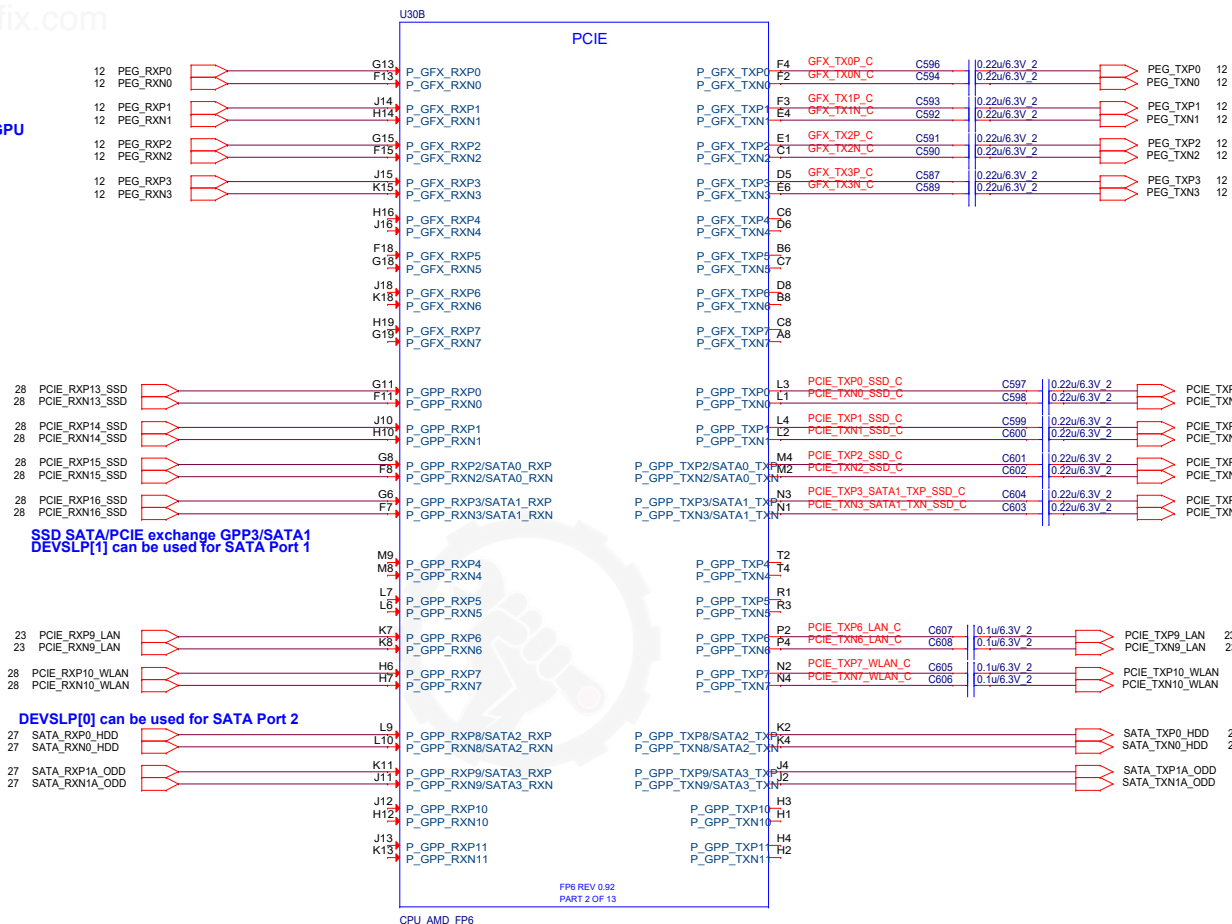
SSD SATA/PCIE exchange GPP3/SATA1  
DEVSLP[1] can be used for SATA Port 1

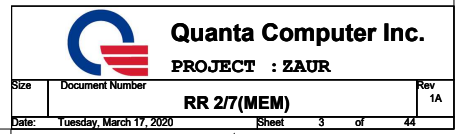
LAN

WLAN

HDD

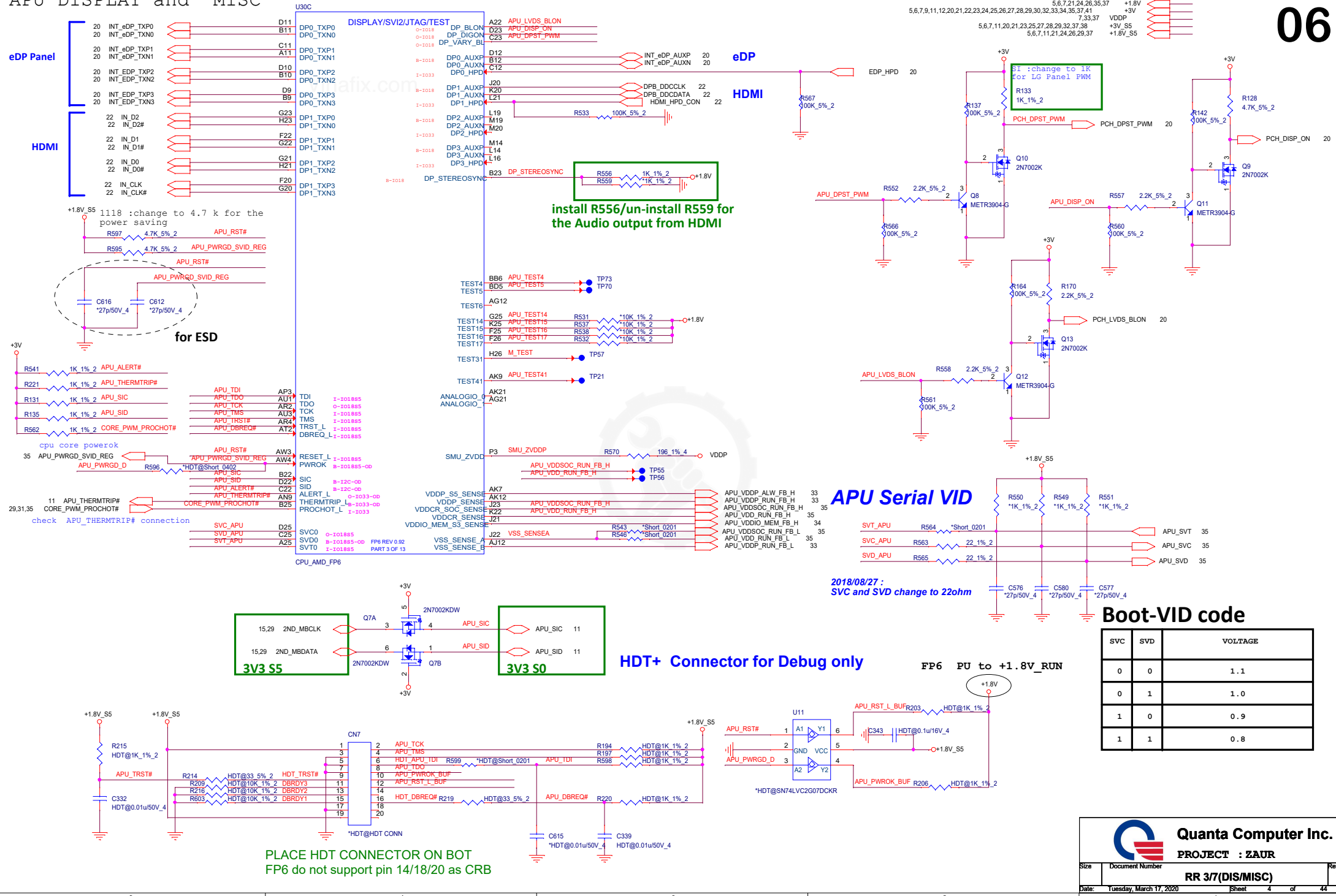
**ODD**



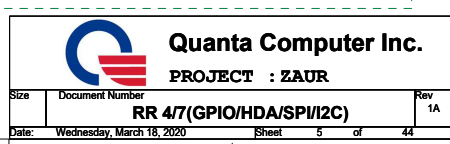


# APU DISPLAY and MISC

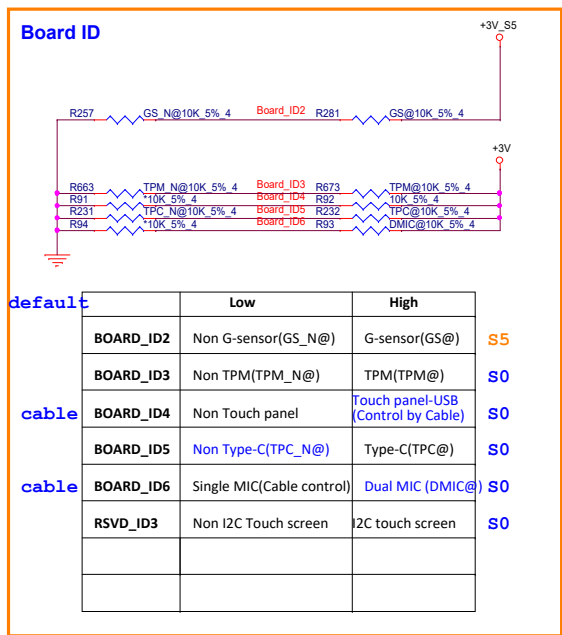
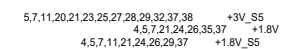
06



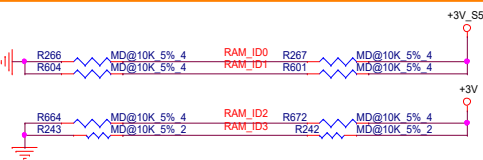
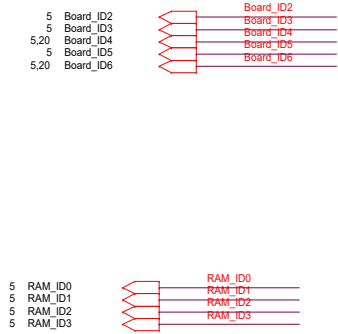
## 07







default	Low	High	
	BOARD_ID2 Non G-sensor(GS_N@)	G-sensor(GS@)	S5
	BOARD_ID3 Non TPM(TPM_N@)	TPM(TPM@)	S0
cable	BOARD_ID4 Non Touch panel	Touch panel-USB (Control by Cable)	S0
	BOARD_ID5 Non Type-C(TPC_N@)	Type-C(TPC@)	S0
cable	BOARD_ID6 Single MIC(Cable control)	Dual MIC (DMIC@)	S0
	RSVD_ID3 Non I2C Touch screen	I2C touch screen	S0

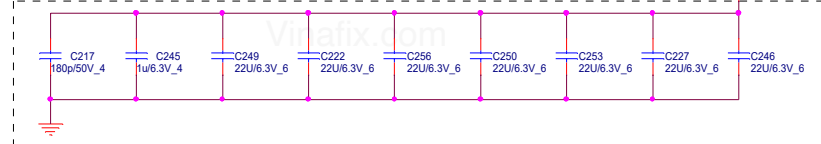


ID3	ID2	ID1	ID0	Vendor	Vendor PN	Quanta PN
0	0	0	0	Hynix 8Gb	H5AN8G6NCJR-KVC	AKD5QGSWTW13
0	0	0	1	Micron 8Gb	MT40A512M16LY-075:E	AKD5LSZTL24
0	0	1	0	Samsung 8Gb	K4A8G165WC-BCTD	AKD5SQGST512
0	0	1	1	Hynix 16Gb	H5ANAG6NCMR-KVC	AKD5RGUTW08
1	1	1	1	Without out on board memory		

# APU POWER

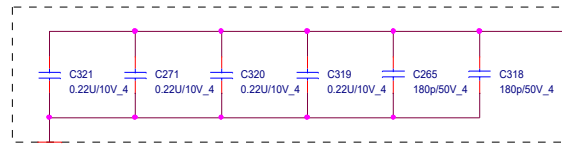
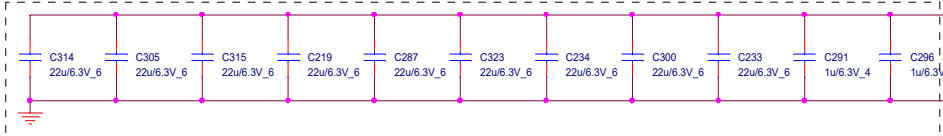
09

## BOTTOM SIDE DECOUPLING UNDER APU



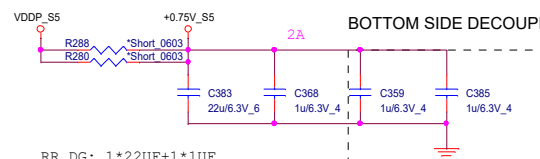
RR DG: 9\*22UF+2\*1UF+4\*0.22uf+3\*180PF

## BOTTOM SIDE DECOUPLING UNDER APU

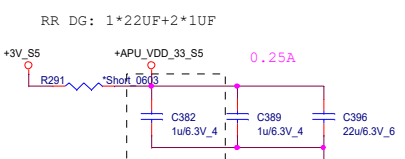


If the VSS plane is cut to create a VDDIO\_MEM\_S3 plane, ceramic capacitors with NP0 or COG dielectric are connected across the VDDIO\_MEM\_S3 and VSS plane split.

RR DG: 1\*22UF+3\*1UF



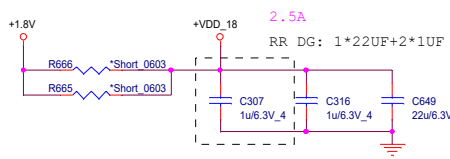
## BOTTOM SIDE DECOUPLING UNDER APU



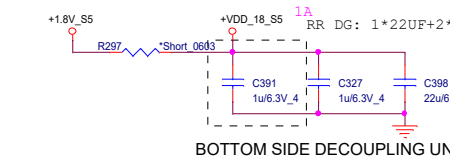
## BOTTOM SIDE DECOUPLING UNDER APU



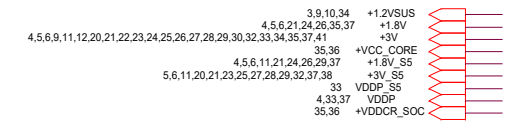
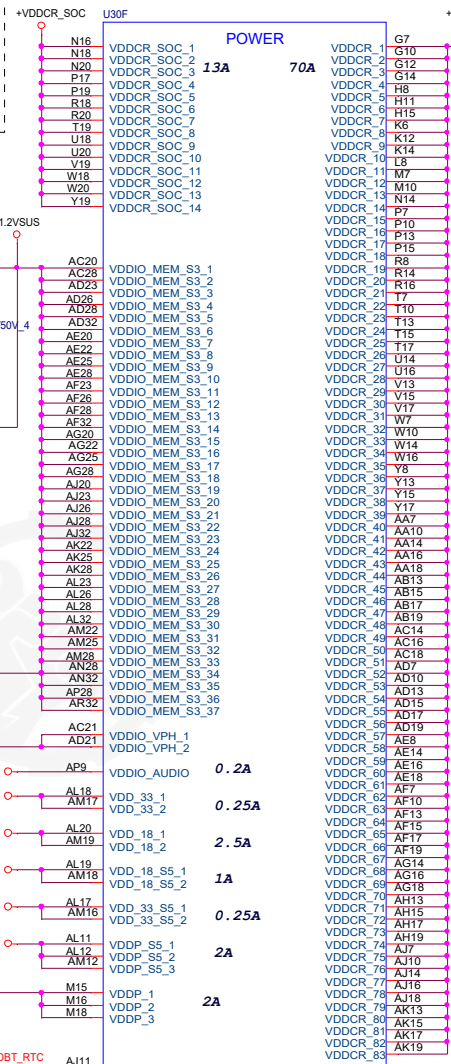
## BOTTOM SIDE DECOUPLING UNDER APU



## BOTTOM SIDE DECOUPLING UNDER APU

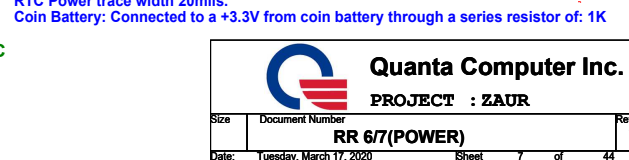
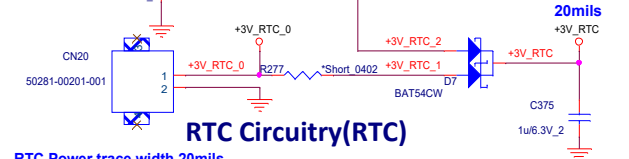
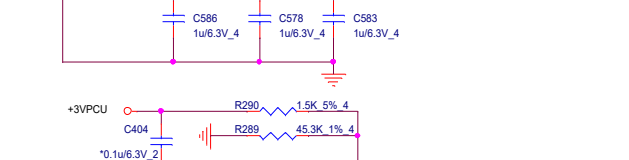
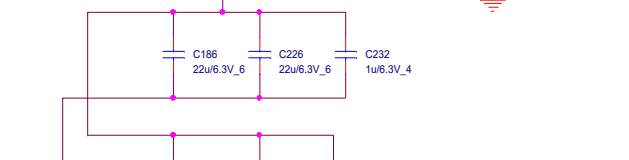
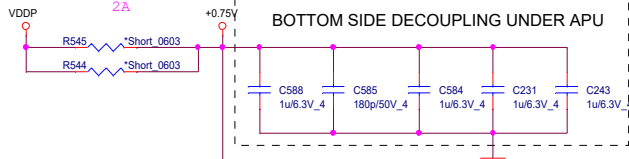
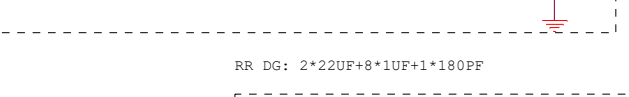


## BOTTOM SIDE DECOUPLING UNDER APU



RR DG: 16\*22UF+1\*180PF

## BOTTOM SIDE DECOUPLING UNDER APU

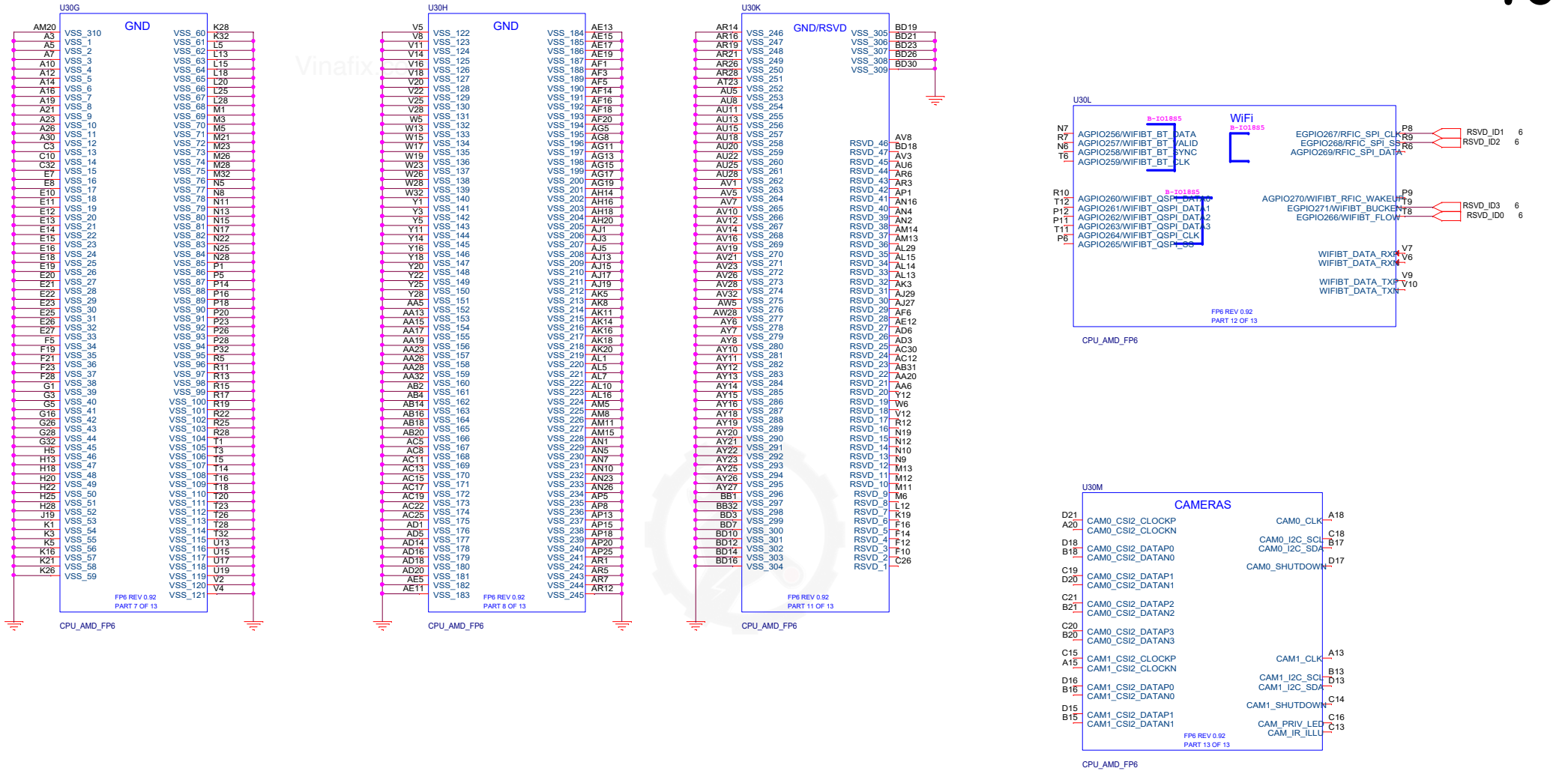


## RTC Circuitry(RTC)

RTC Power trace width 20mils. Coin Battery: Connected to a +3.3V from coin battery through a series resistor of: 1K

**Quanta Computer Inc.**  
PROJECT : ZAUR

Size	Document Number	Rev
	<b>RR 67(POWER)</b>	1A
Date:	Tuesday, March 17, 2020	Sheet 7 of 44



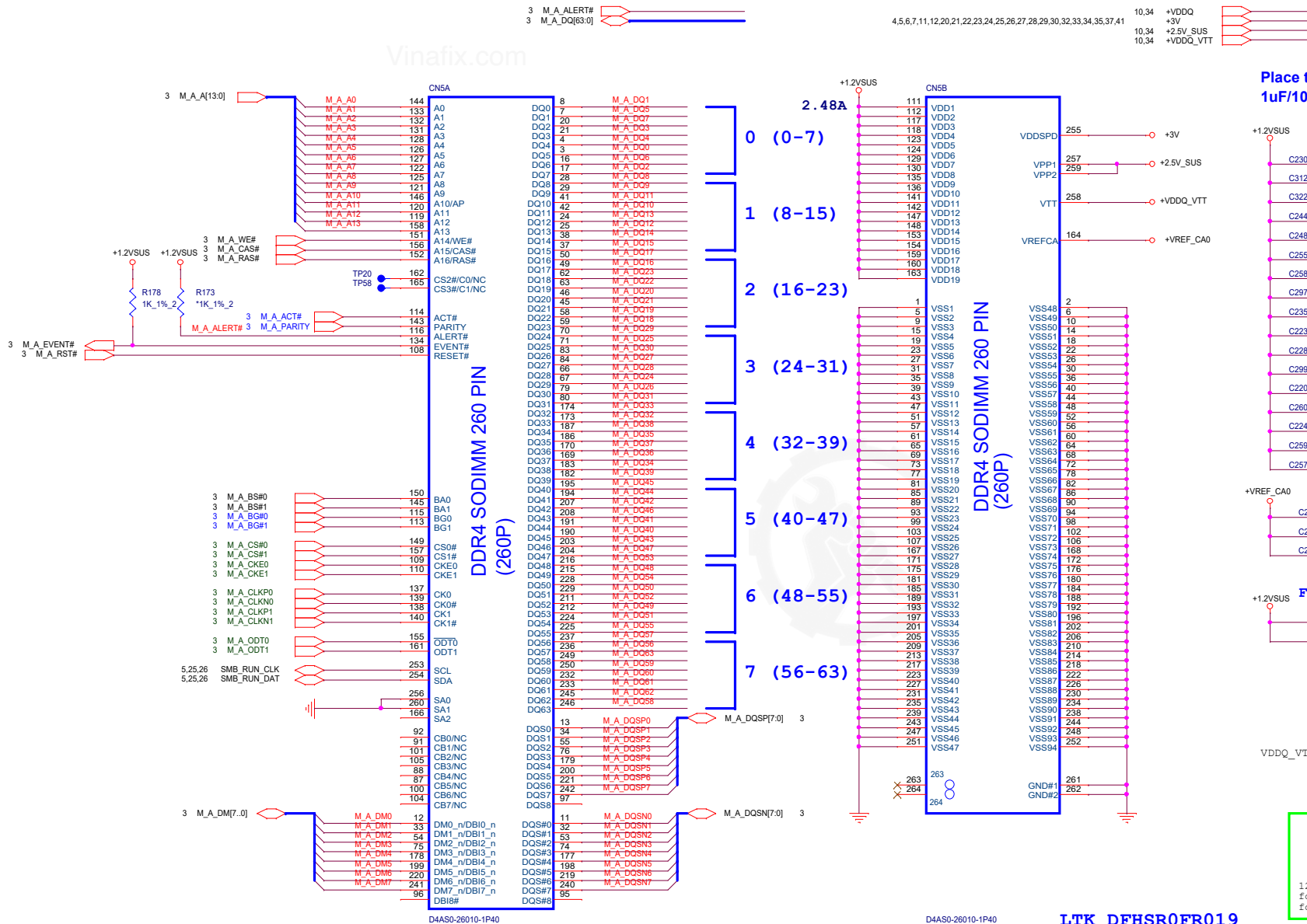
Quanta Computer Inc.

PROJECT : ZAUR

Size	Document Number	Rev
	RR 77(GND/RSVD)	1A

Date: Tuesday, March 17, 2020 Sheet 8 of 44

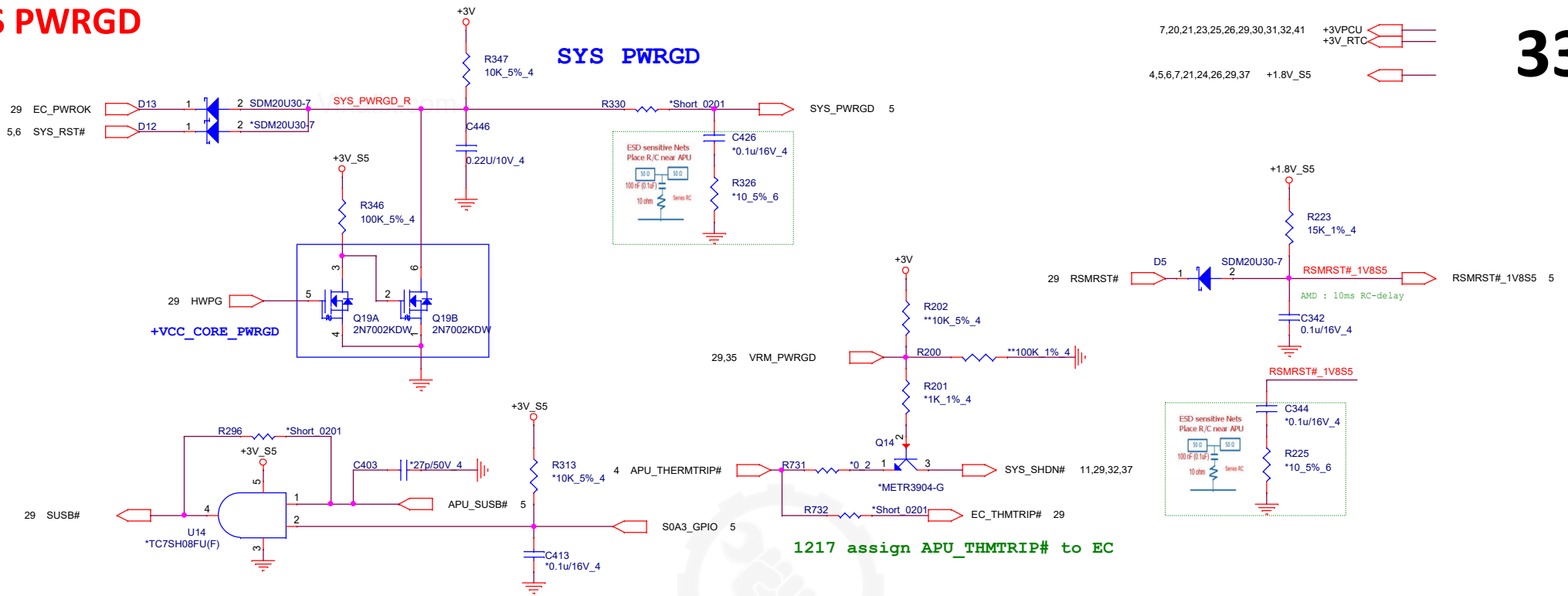




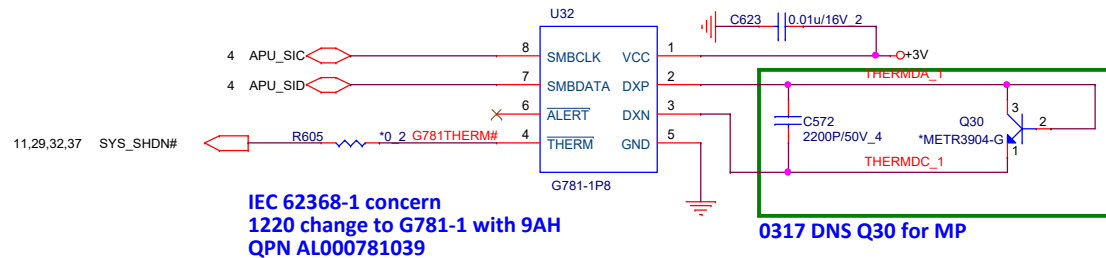


# SYS\_PWRGD

## SYS\_PWRGD



## Address 9AH



Quanta Computer Inc.

PROJECT : ZAUR

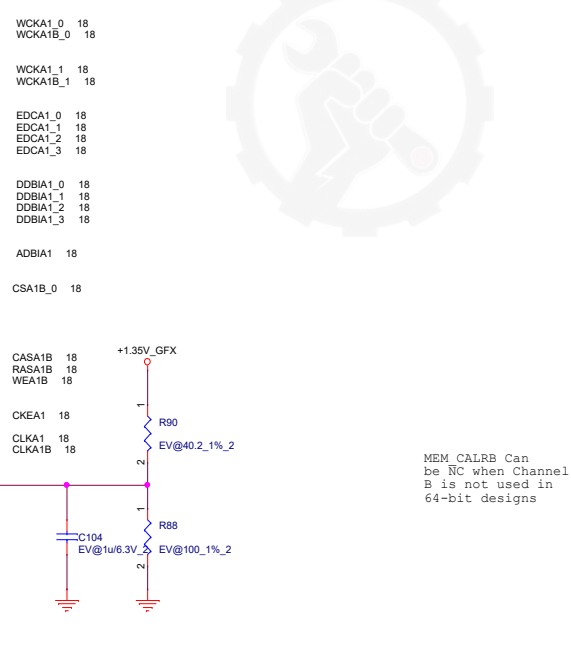
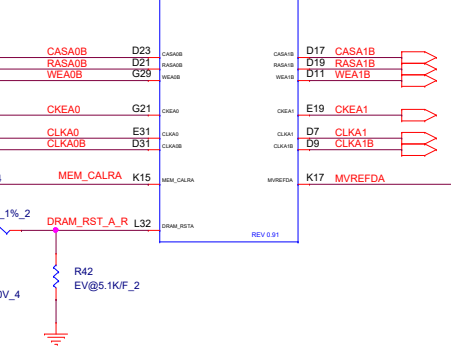
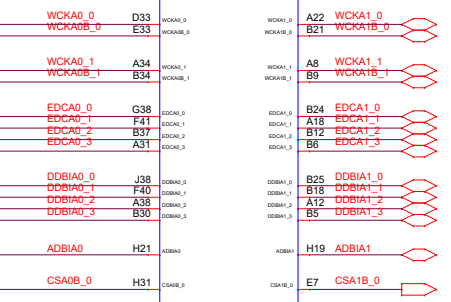
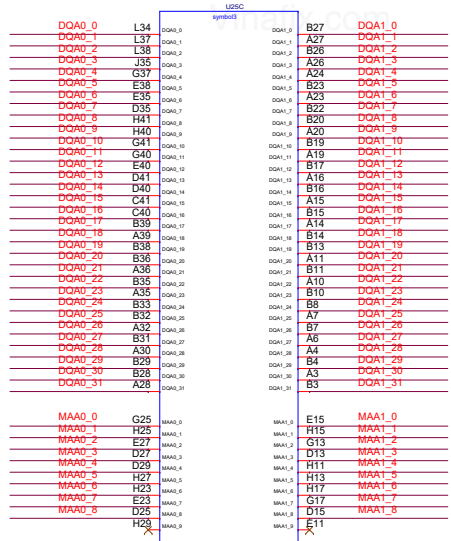
Size	Document Number	Rev
	RR SYSPWRGD/ThermalSensor	1A

Date: Tuesday, March 17, 2020 Sheet 11 of 44

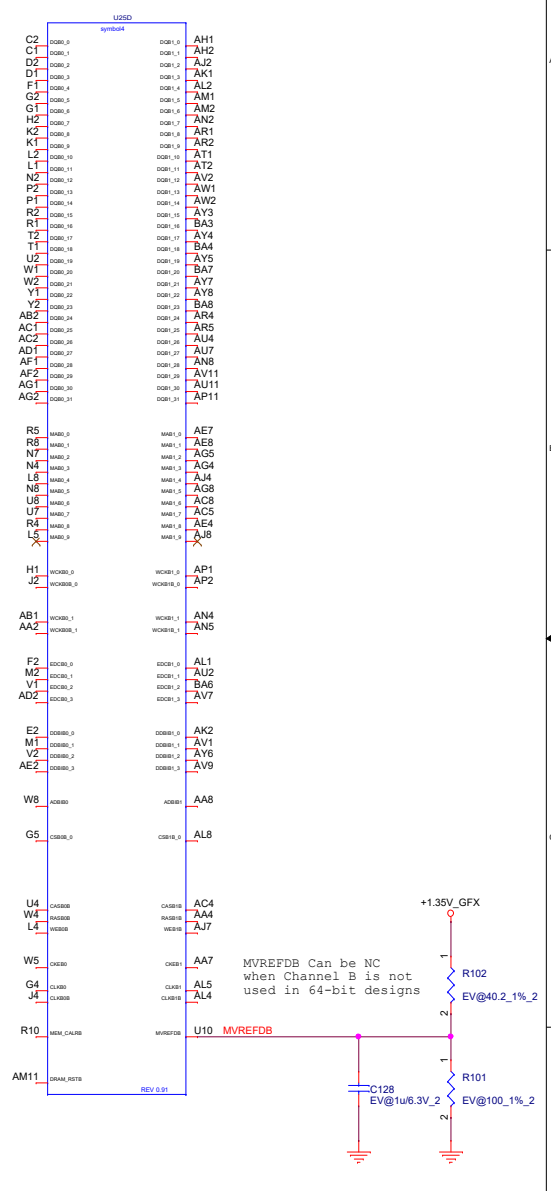


18 DQA0\_[31:0] 18  
18 MAA0\_[8:0] 18

DQA1\_[31:0] 18  
MAA1\_[8:0] 18

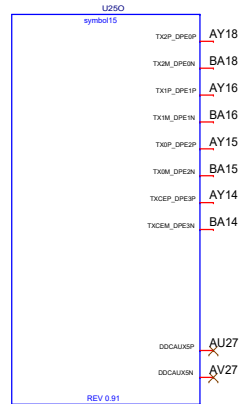


MEM CALRB Can be NC when Channel B is not used in 64-bit designs

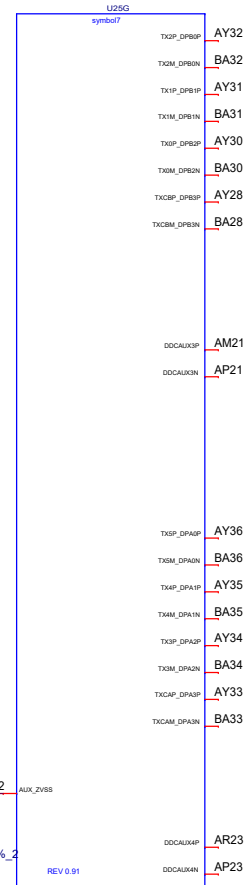




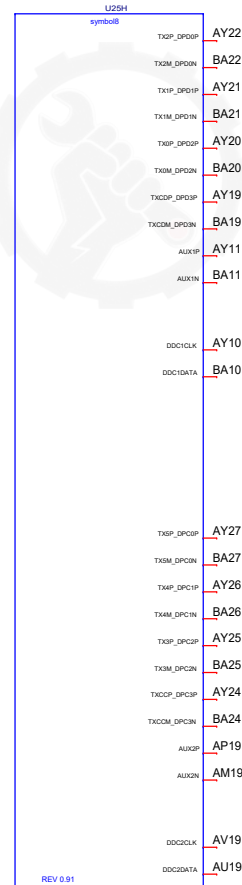
# ASIC - TMDP (E)

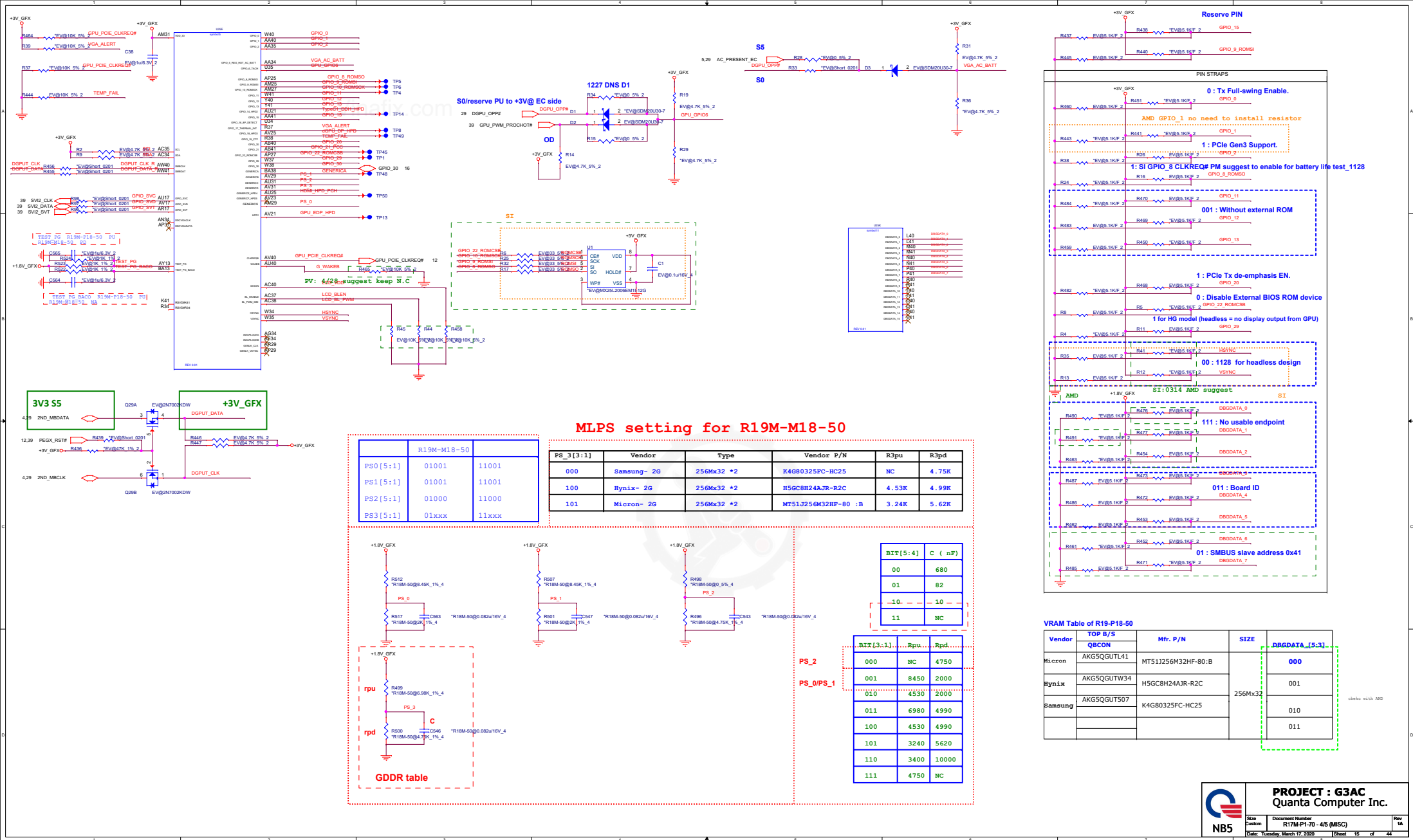


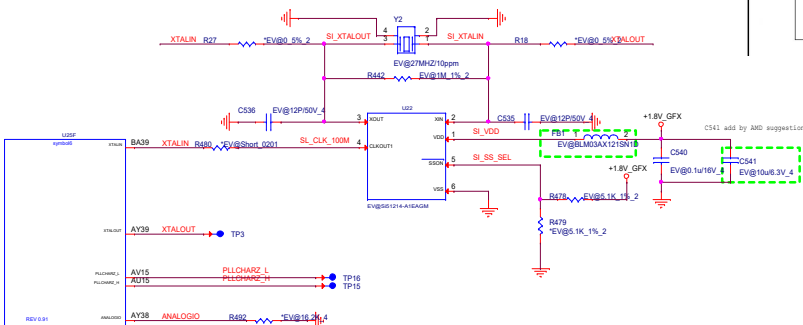
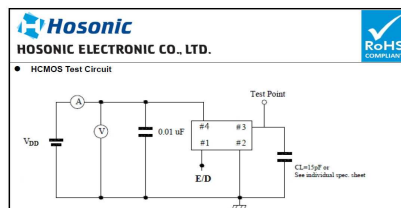
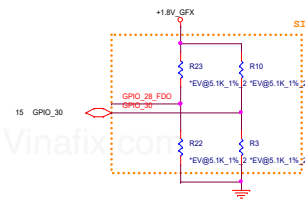
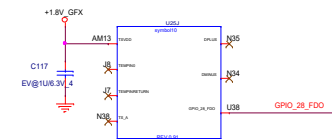
# ASIC - TMDP (A/B)



# ASIC - TMDP (C/D)

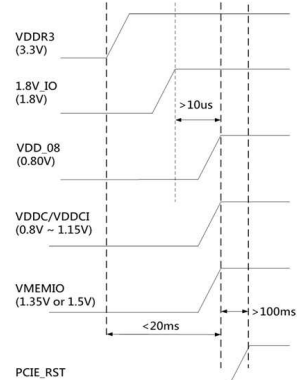




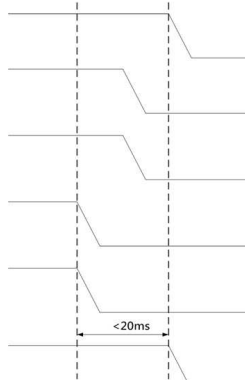


R10M-G1-10 Power up sequence for you refer:

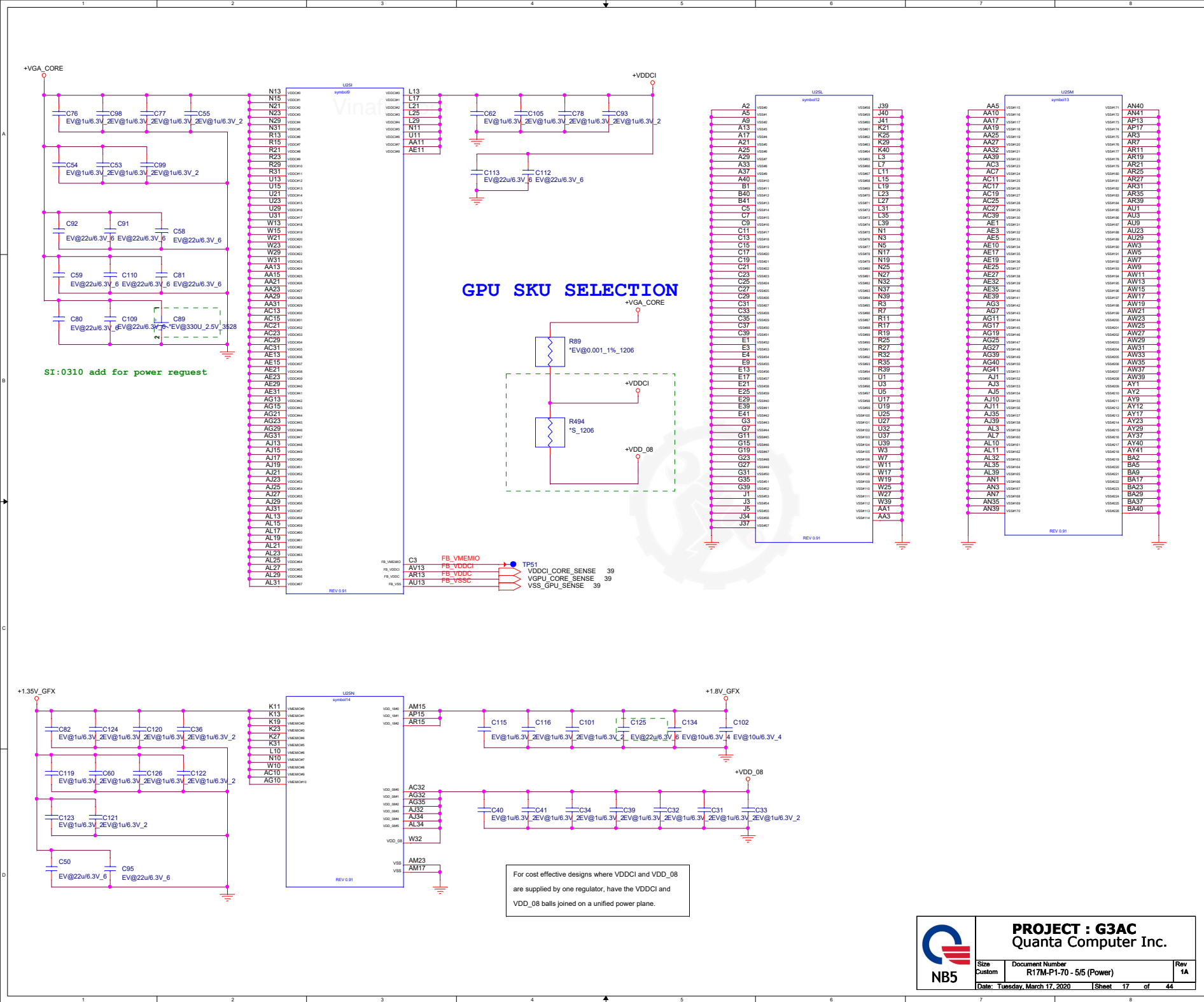
## POWER UP



## POWER DOWN



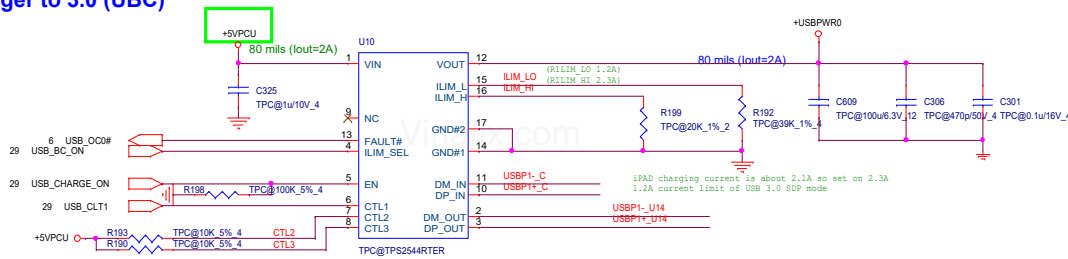
AMD GPIO Strapping	Setting	Name	Description
GPIO 29	Pull low 10K ohm	BIF_VGA_DIS	0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).
GPIO 20	Pull up 10K ohm	TX_DEEMPH_EN	PCI Express transmitter deemphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.
GPIO 0	Pull up 10K ohm	TX_HALF_SWING	Controls the transmitter full/half swing mode. 0: The transmitter full swing is enabled. 1: The transmitter half swing is enabled.
GPIO 22	Pull low 10K ohm	BIOS_ROM_EN	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device.
GPIO 11	Pull up 10K ohm	ROM_CONFIG[2:0]	b) If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. GPIO_13[2:11]=001=256MB
GPIO 12	Pull low 10K ohm		
GPIO 13	Pull low 10K ohm		
Hsync	NC	Reserve	Reserve
Vsync	NC		
DBGDATA2	Pull up 10K ohm	AUD_PORT_CONN[2:0]	Determine the maximum number of digital display audio endpoints 101: Two usable endpoints
DBGDATA1	Pull low 10K ohm		
DBGDATA0	Pull up 10K ohm		
GPIO 1	Pull up 10K ohm	SMBUS_ADDR	Provide a strap option to change the SMBUS slave address of the GPU. 0: 0x40 1: 0x41
GPIO 2	Pull up 10K ohm	BIF_GEN3_EN_A	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.
GPIO 8	connect CLKREQ#_GPU and add pull up / down resistor	BIF_CLK_PM_EN (Reserve)	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.
WAKEB	Pull low 10K ohm	OBFF	0: Disable
SVI2_SVC	Pull up 1Kohm	Boot up voltage	SVC:SVDD[1:0]=0.90V
SVI2_SVD	Pull low 1K ohm		







USB Charger to 3.0 (UBC)

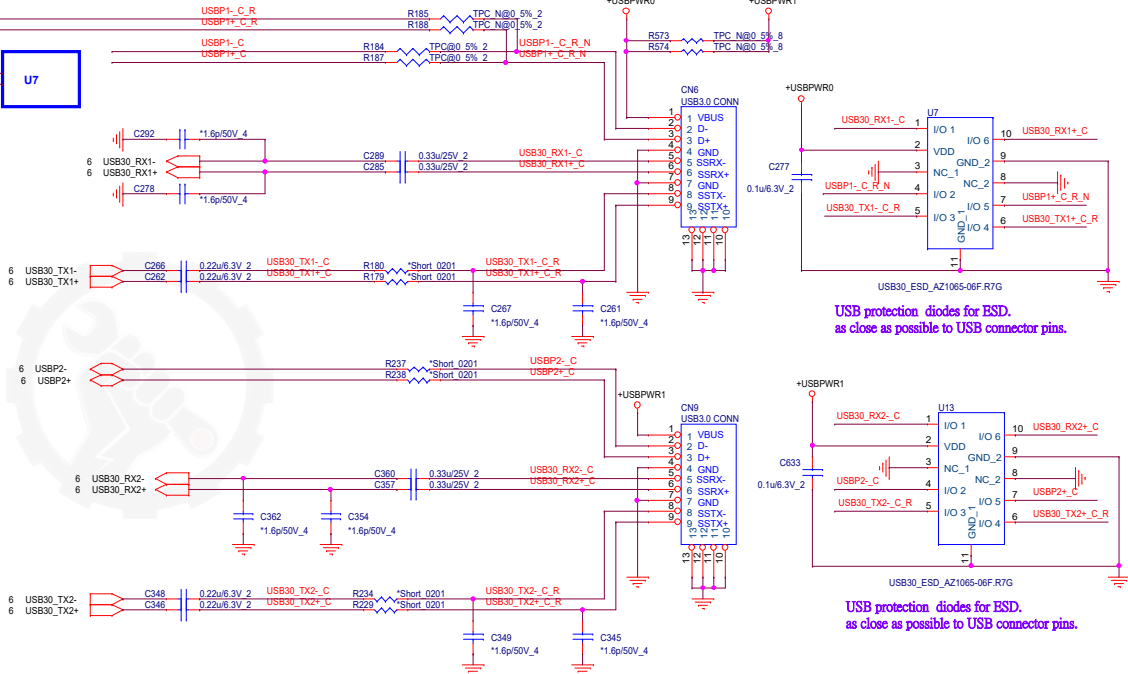
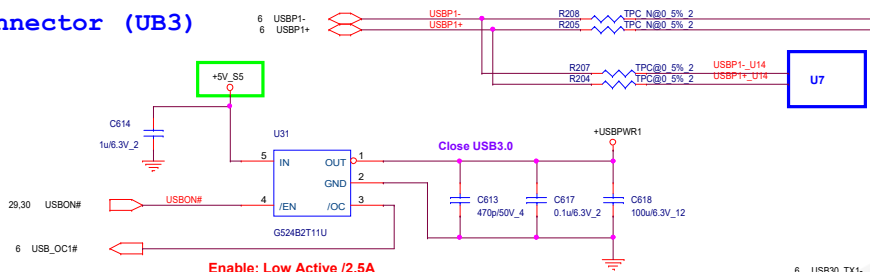


	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

0326 TI AL002544001 (TPS2544RTER)

RILIM\_LO is optional and the ILIM\_LO pin may be left unconnected if the following conditions are met:  
1. ILIM\_SEL is always set high  
2. Load Detection - Port Power Management is not used  
3. Mouse / Keyboard wake function is not used  
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM\_LO < 80.6 kΩ.  
The following equation programs the typical current limit:  
(1)  $I_{OS\_typ}(mA) = 50,250 / \{RILIM\_XX(K\Omega) + 0.1\}$   
RILIM\_XX corresponds to either RILIM\_HI or RILIM\_LO as appropriate.

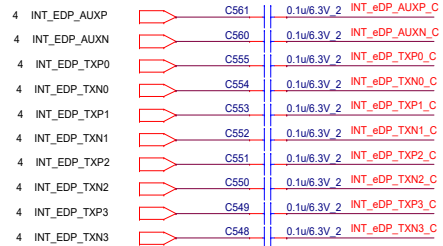
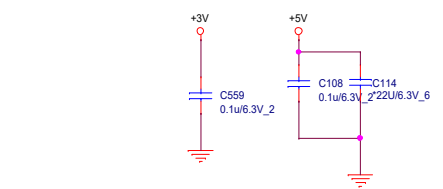
USB 3.0 Connector (UB3)



USB protection diodes for ESD, as close as possible to USB connector pins.

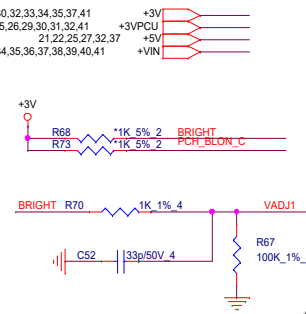
USB protection diodes for ESD, as close as possible to USB connector pins.

CAP close to different CONN

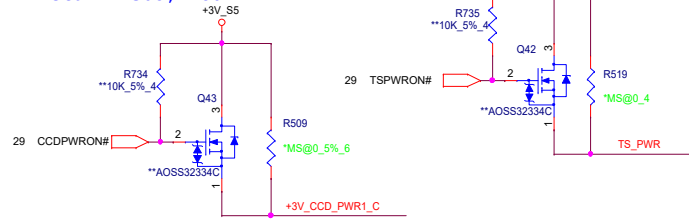


4,5,6,7,9,11,12,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,41  
7,21,23,25,26,29,30,31,32,41  
21,22,25,27,32,37  
31,32,33,34,35,36,37,38,39,40,41

Vinafix.com



1220 reserve for MS  
1227 remove MS CCD/TS power rail=S0  
stuff R508, R80

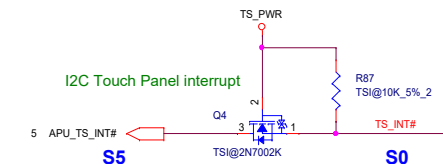


## LCD back light

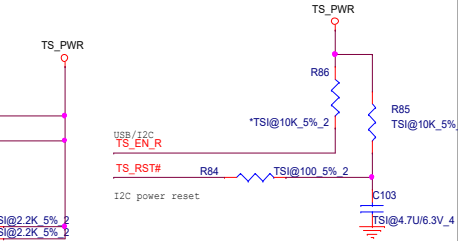
## PCH

## EC

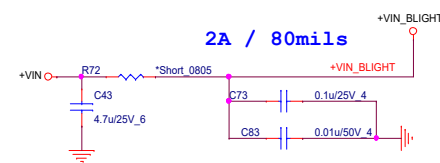
## HID-I2C Touch screen



TP\_SCL, TP\_SDA  
Open Drain,  
Pull high 2.2Kohm

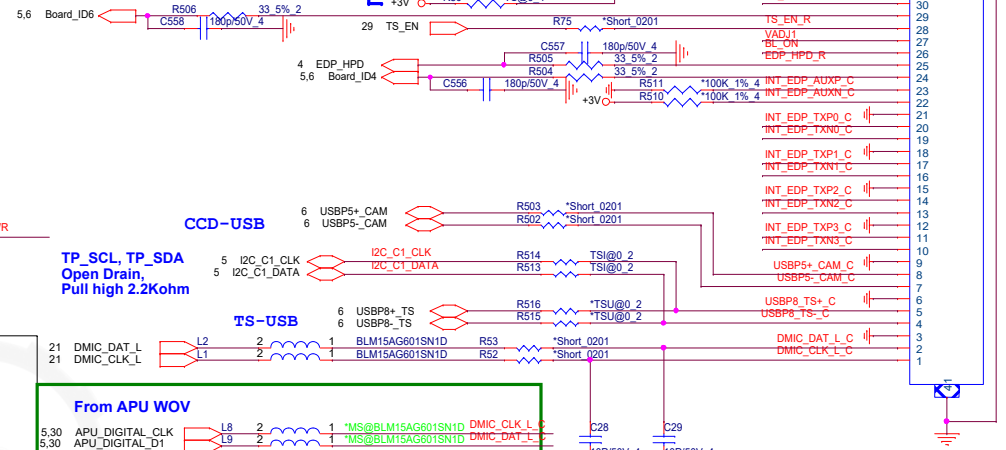


2A / 80mils



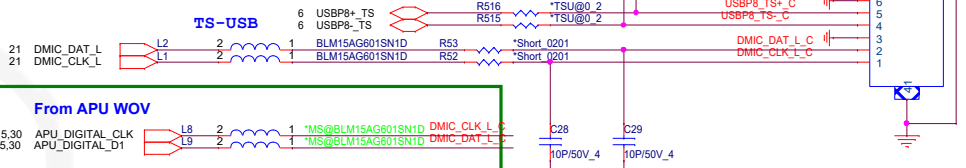
## eDP Conn.

## CCD MIC POWER TouchScreen POWER



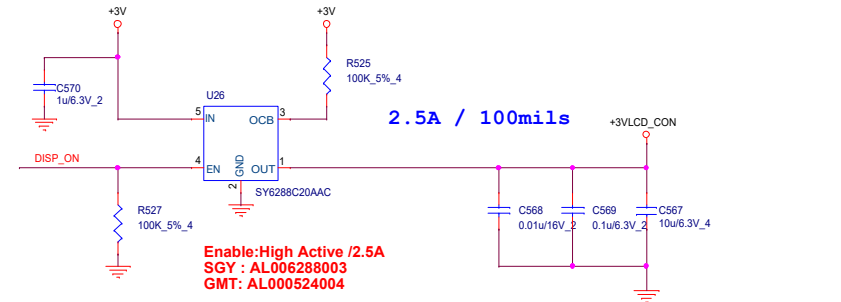
## CCD-USB

TP\_SCL, TP\_SDA  
Open Drain,  
Pull high 2.2Kohm



From APU WOV

1227 remove WOV, stuff R52, R53



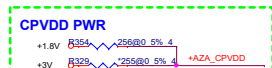
Enable:High Active /2.5A  
SGY : AL006288003  
GMT: AL000524004



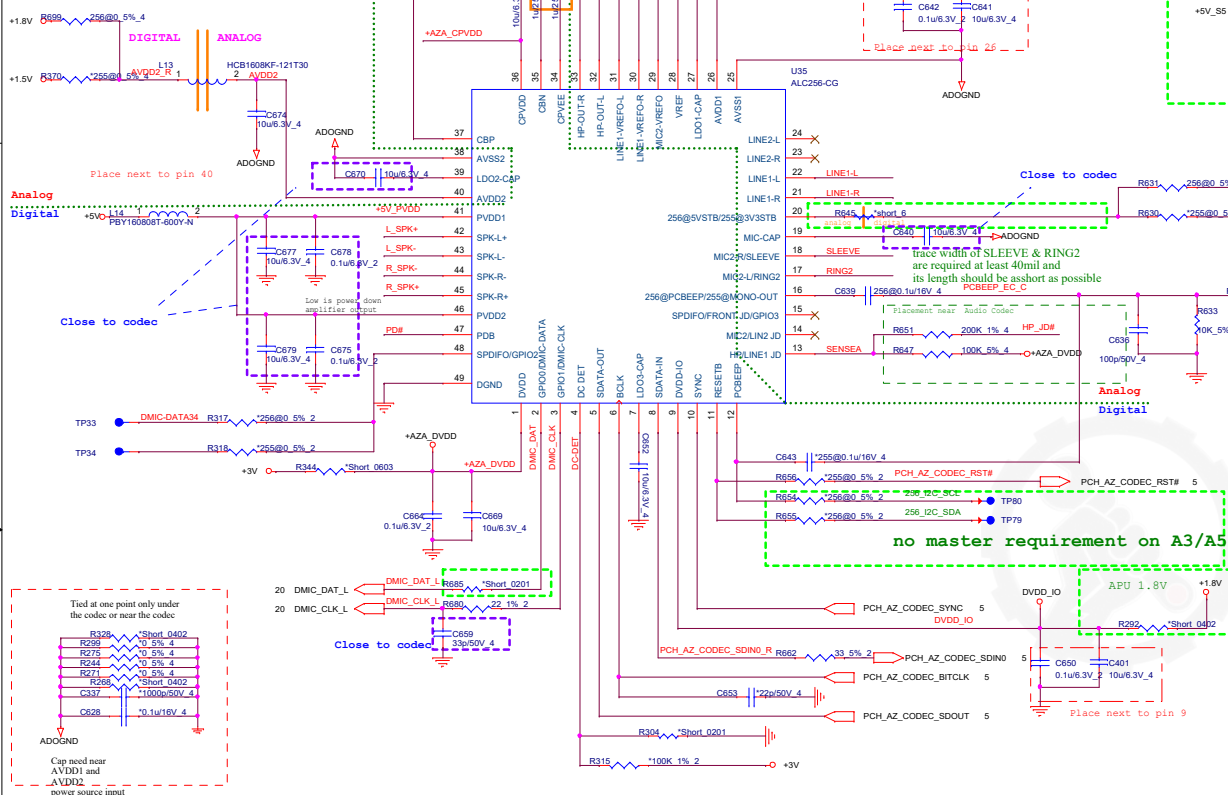
Quanta Computer Inc.  
PROJECT : ZAUR

Size	Document Number	Rev
	eDP CONN/LID/CAM/D-MIC/TS	1A
Date:	Wednesday, March 18, 2020	Sheet 20 of 44

## Codec(ADO)



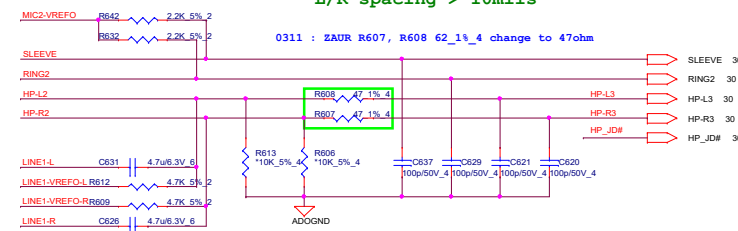
### Codec PWR 1.8V(ADO)



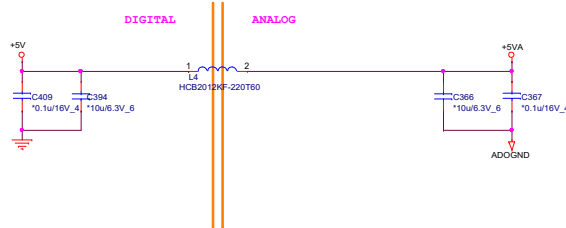
WW G2 @ ALC256 : AL000256009  
MGF G3 @ ALC3256M:  
ALC255 : AL000255000- Design reserved

**Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)**

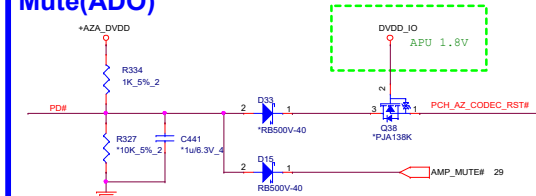
SLEEVE/RING2 trace > 40mils  
HP/LINE trace > 10mils  
L/R spacing > 10mils



### Codec PWR 5V(ADO)



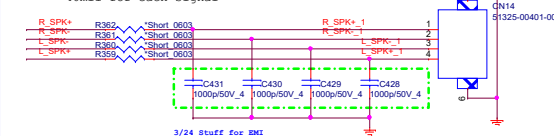
## Mute(ADO)

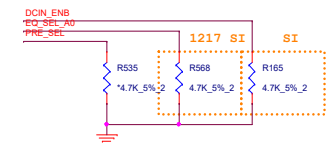


## Internal Speaker

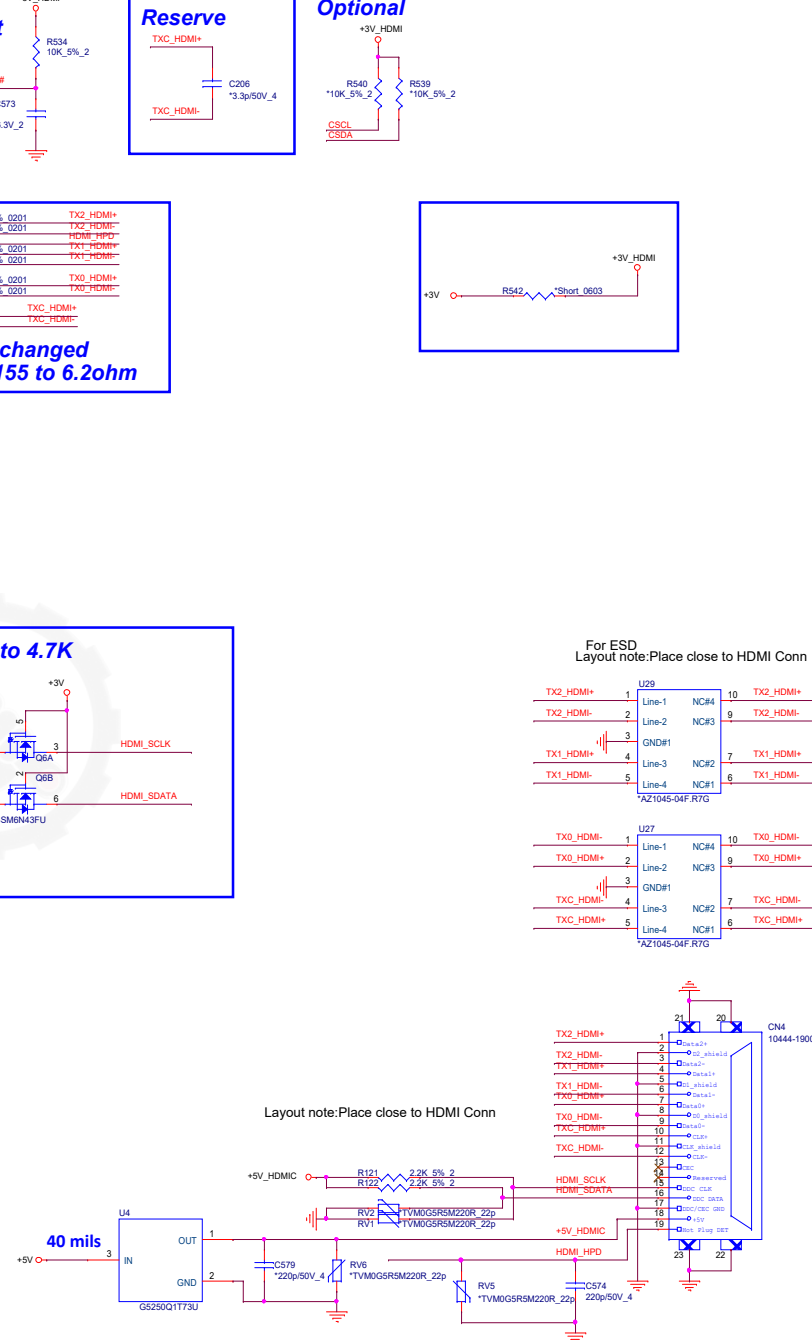
4 ohm : 40mil for each signal

40mil for each signal



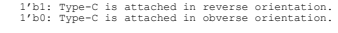


```
I2C_SEL_PIN
I2C Slave Address selection; Internal pull down, 3.3V I/O.
L: Default, Slave address 0x10-0x2F.
H: Alternative slave address 0x90-0x9F, 0xD0-0xDF.
```

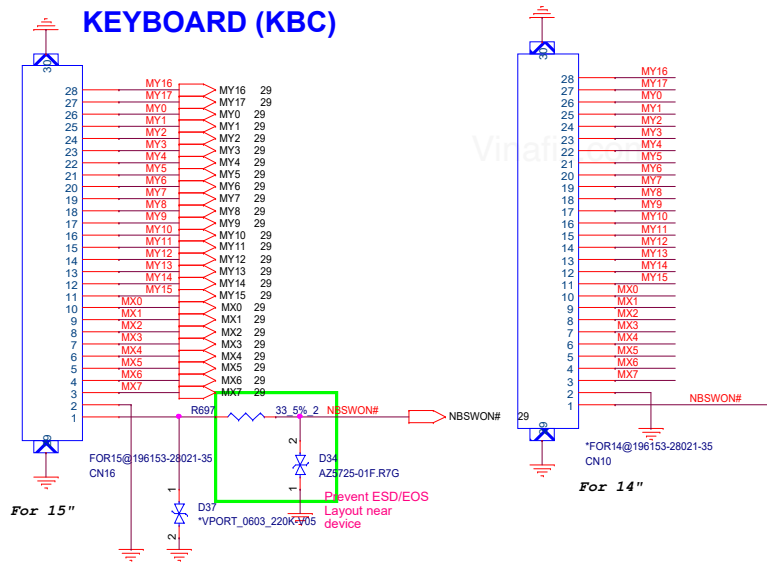






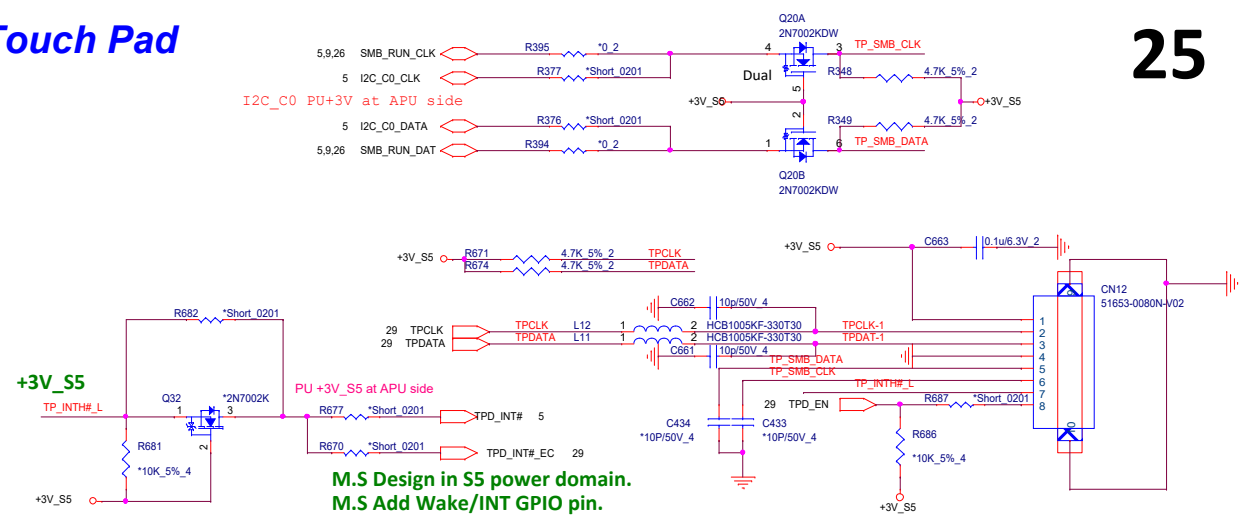


## KEYBOARD (KBC)

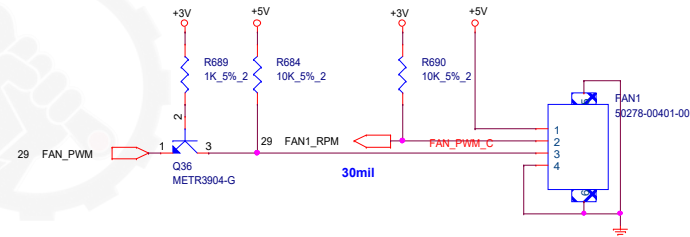


MY5	C468	220p/25V_2
MY6	C469	220p/25V_2
MY3	C466	220p/25V_2
MY7	C470	220p/25V_2
MY8	C471	220p/25V_2
MY9	C472	220p/25V_2
MY10	C473	220p/25V_2
MY11	C474	220p/25V_2
MY1	C464	220p/25V_2
MY2	C465	220p/25V_2
MY4	C467	220p/25V_2
MY0	C463	220p/25V_2
MX4	C688	220p/25V_2
MX6	C690	220p/25V_2
MX5	C687	220p/25V_2
MX2	C686	220p/25V_2
MX7	C691	220p/25V_2
MX0	C684	220p/25V_2
MX5	C689	220p/25V_2
MX1	C685	220p/25V_2
MY12	C475	220p/25V_2
MY13	C476	220p/25V_2
MY14	C477	220p/25V_2
MY15	C683	220p/25V_2
MY16	C461	220p/25V_2
MY17	C462	220p/25V_2

## Touch Pad

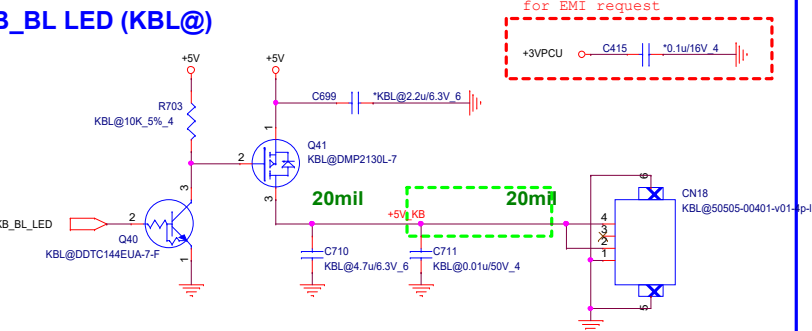


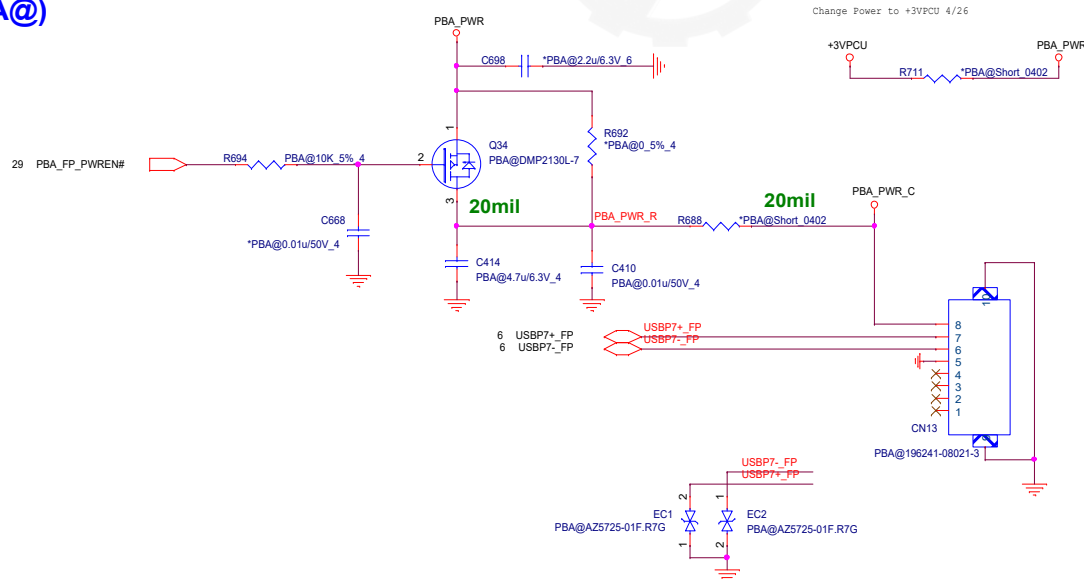
## FAN



25

## KB\_LED (KBL@)



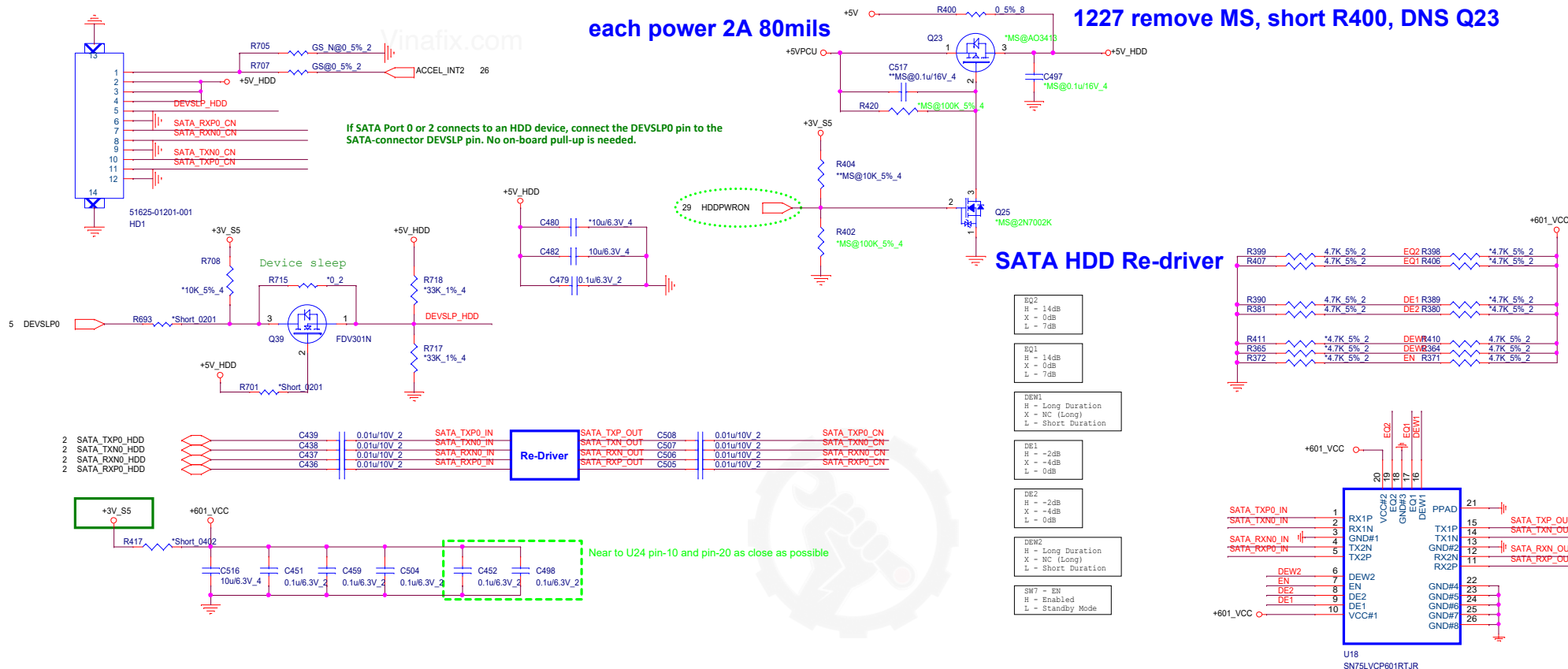


M.S SATA SSD devices should be powered from S5 rail during S0i3, and should support DEVSLP as well as HIPM functionality. The SATA SSD power should be gated by EC GPIO during S3, S4, and S5.

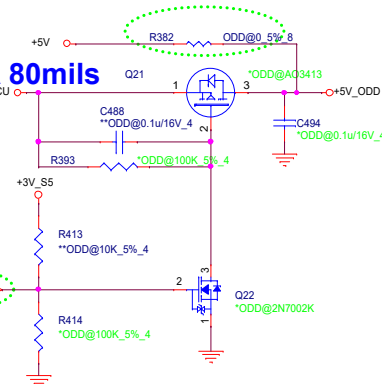
	19,21,24,30,32,34,35,39	+5V_S5
	20,21,22,25,32,37	+5V
4,5,6,7,9,11,12,20,21,22,23,24,25,26,28,29,30,32,33,34,35,37,41		+3V
	5,6,7,11,20,21,23,25,28,29,32,37,38	+3V_S5



27



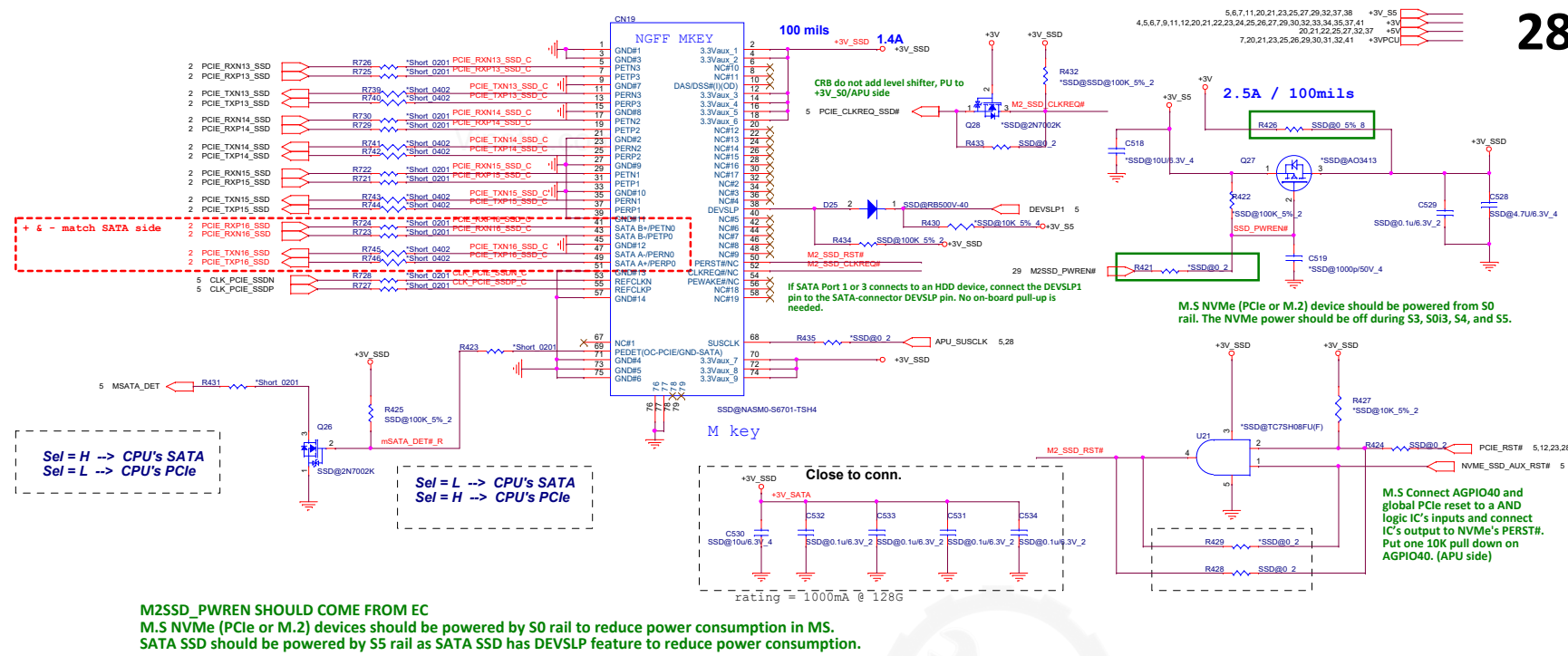
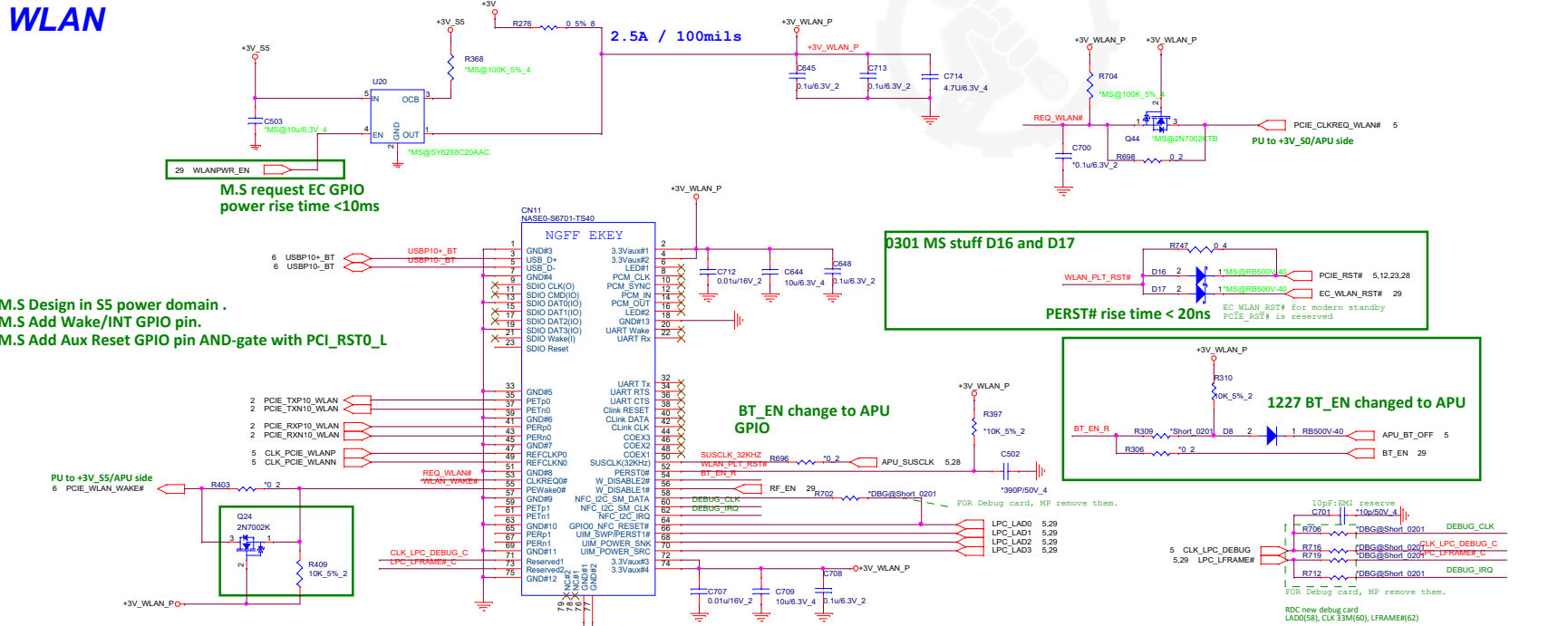
M.S EC assignment reserved  
A3/A5 do not support ODD

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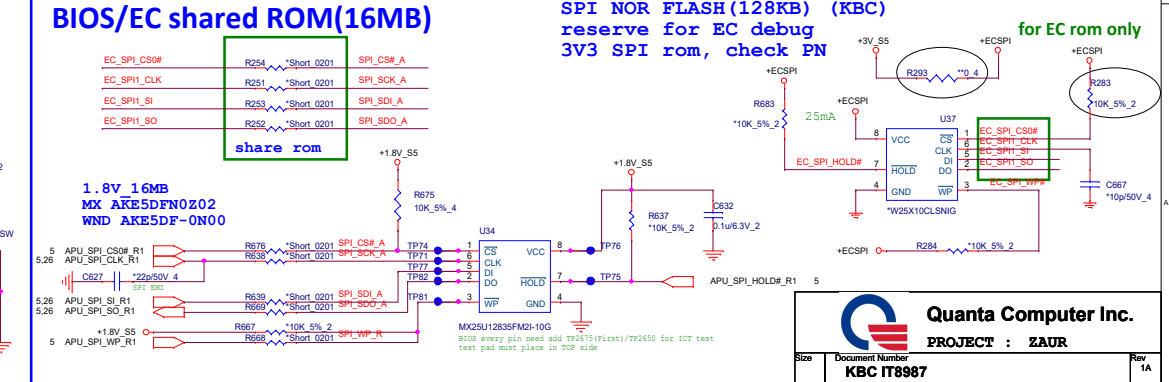
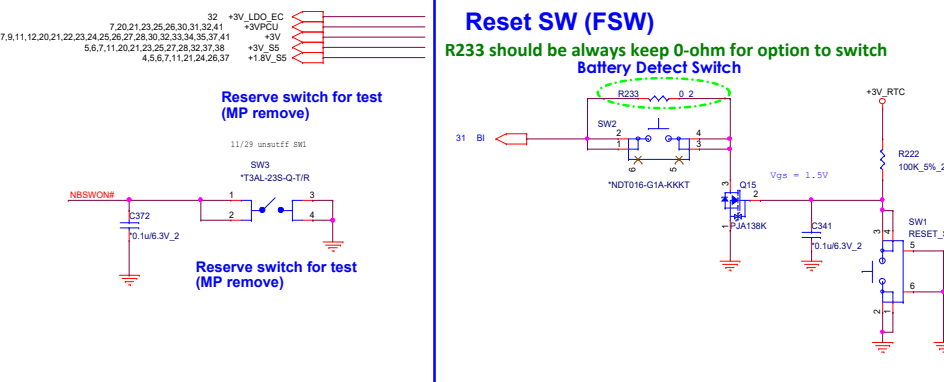
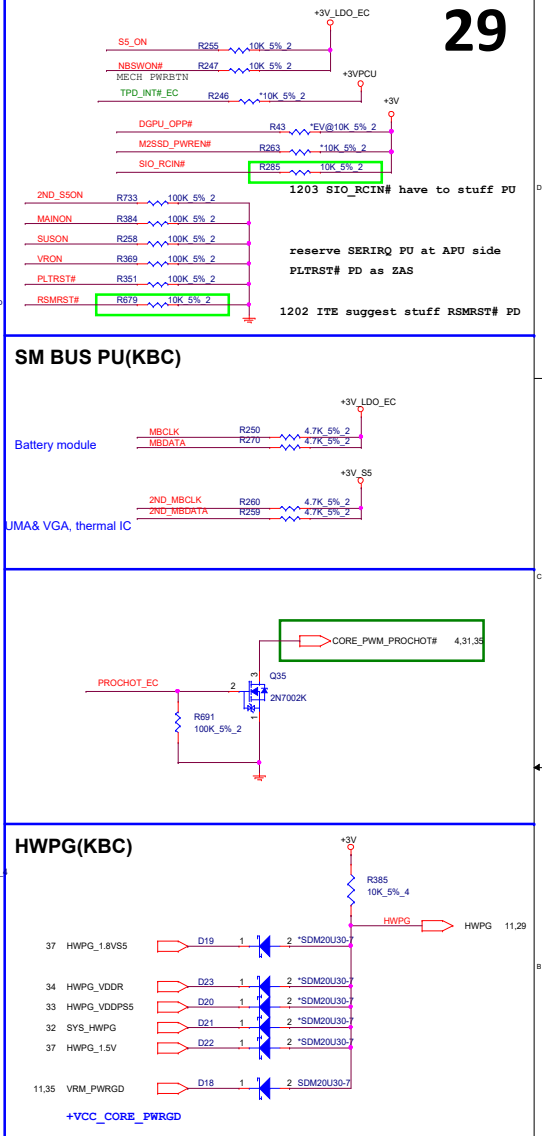
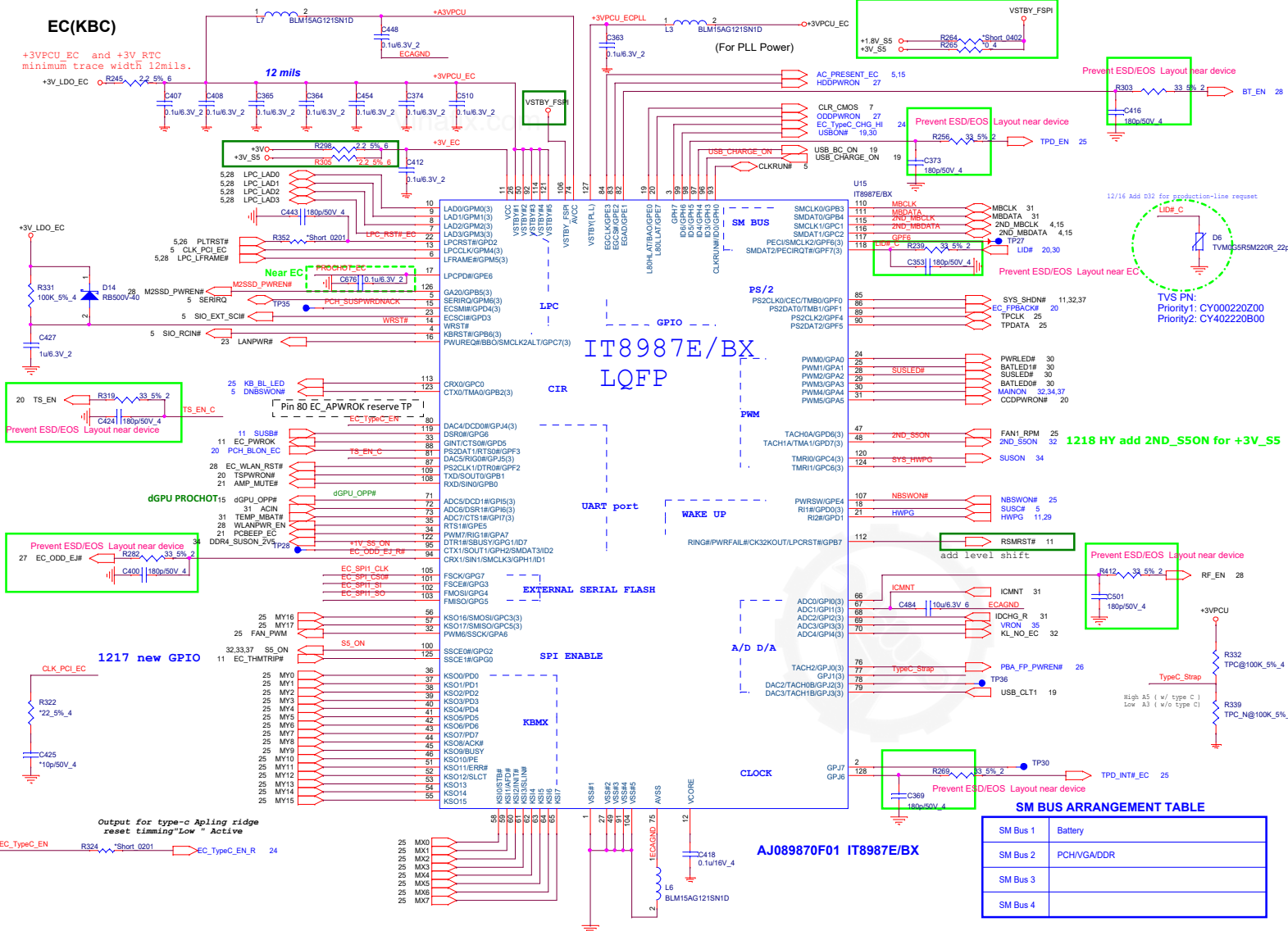
**PROJECT : ZAUR**

Size	Document Number	Rev
	<b>HDD/ ODD</b>	1A
Date:	Tuesday, March 17, 2020	Sheet 27 of 44

5,6,7,11,20,21,23,25,27,29,32,37,38 +3V\_S5  
4,5,6,7,9,11,12,20,21,22,23,24,25,26,27,29,30,32,33,34,35,37,41 +3V  
20,21,22,25,27,32,37 +5V  
7,20,21,23,25,26,29,30,31,32,41 +3VPCU

**WLAN**

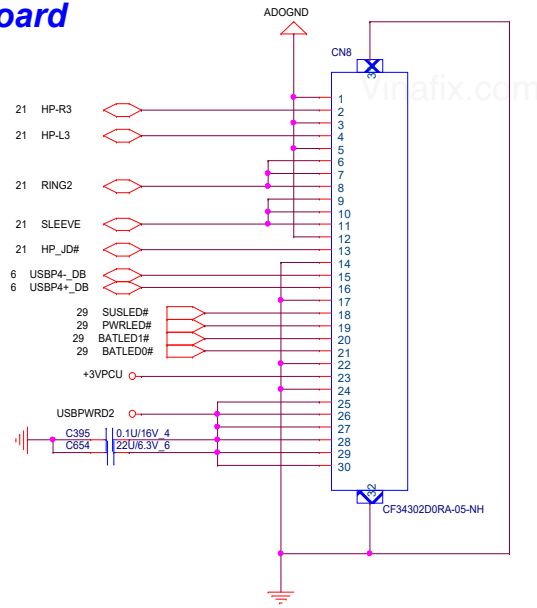
**EC(KBC)**



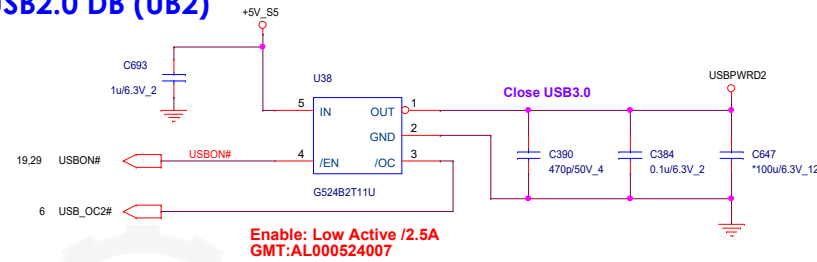


## USB Board

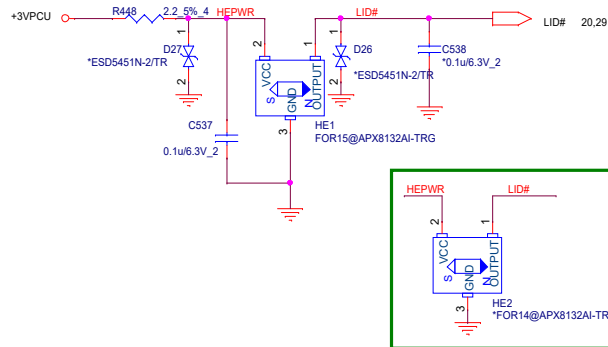
30



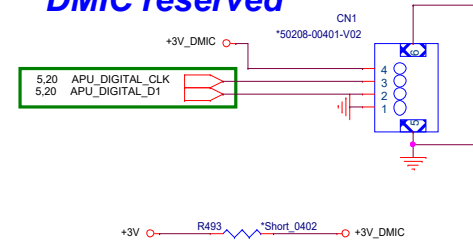
## USB2.0 DB (UB2)



## Hall Sensor



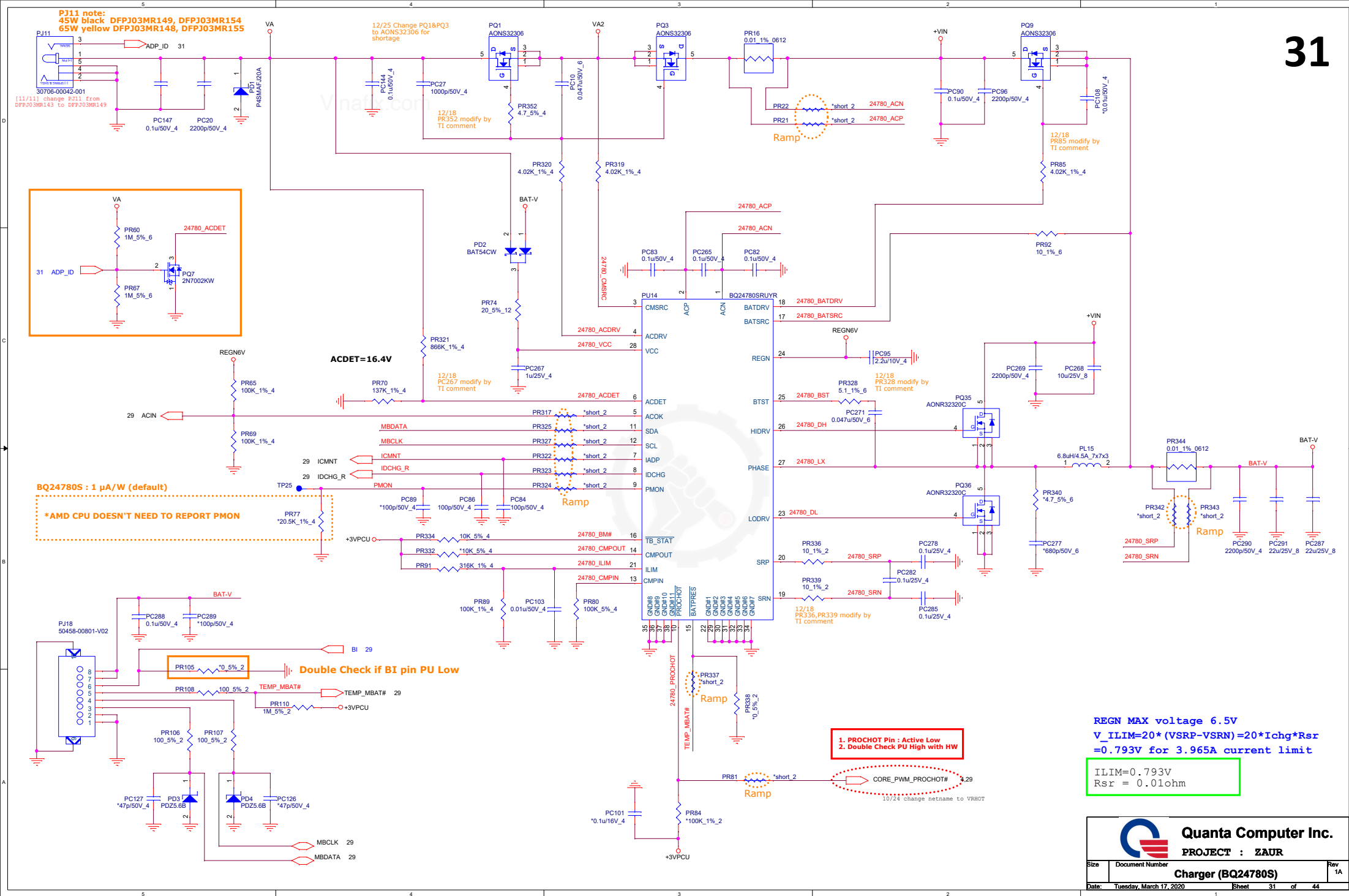
## DMIC reserved



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PROJECT : ZAUR

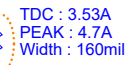
Size	Document Number	Rev
	USB DB/Hall sensor/DMIC	1A
Date:	Tuesday, March 17, 2020	Sheet 30 of 44

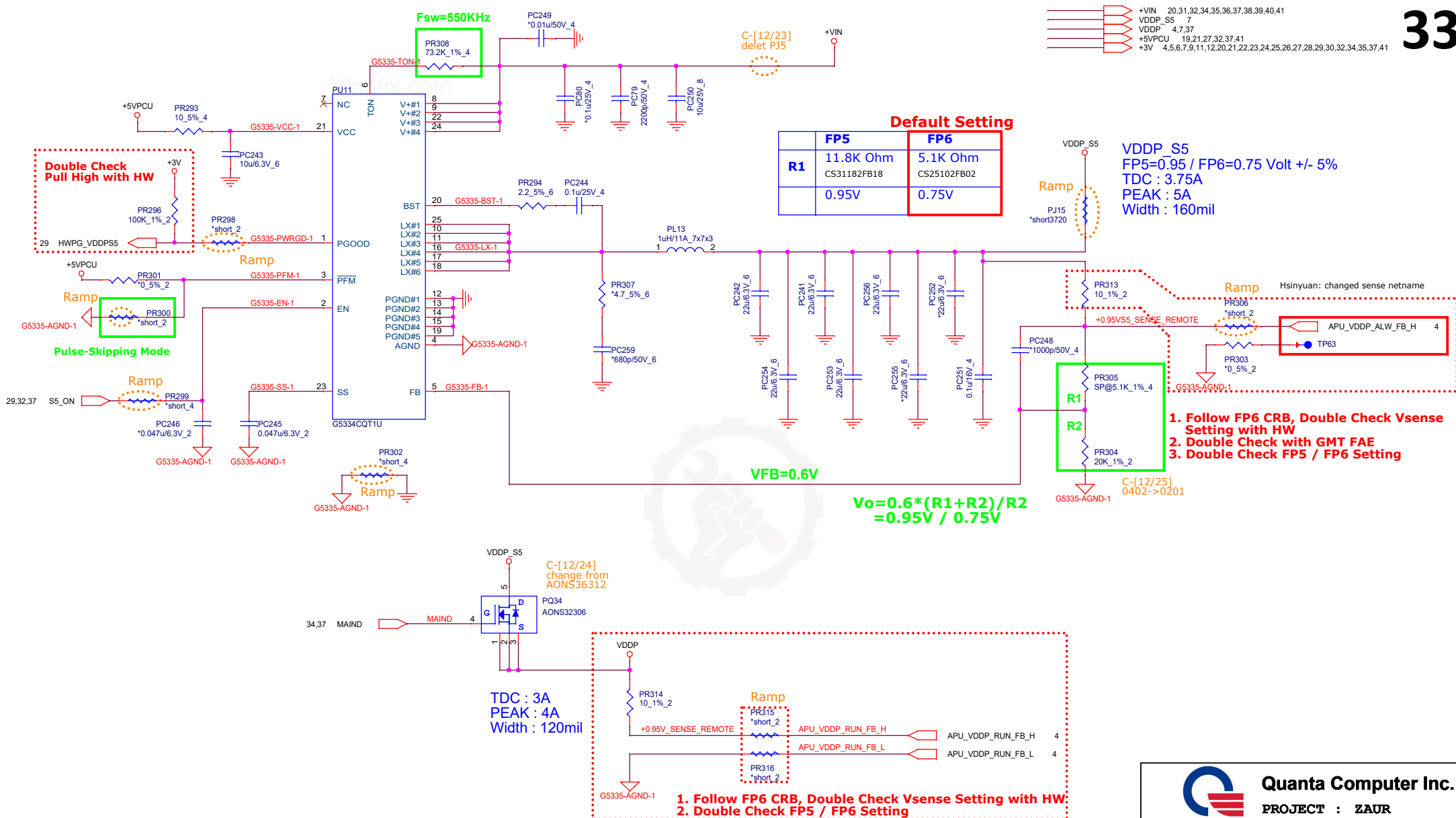




+VIN	20,31,33,34,35,36,37,38,39,40,41
+3VPCU	7,20,21,23,25,26,29,30,31,41
+5VPCU	19,21,27,33,37,41
VL	37

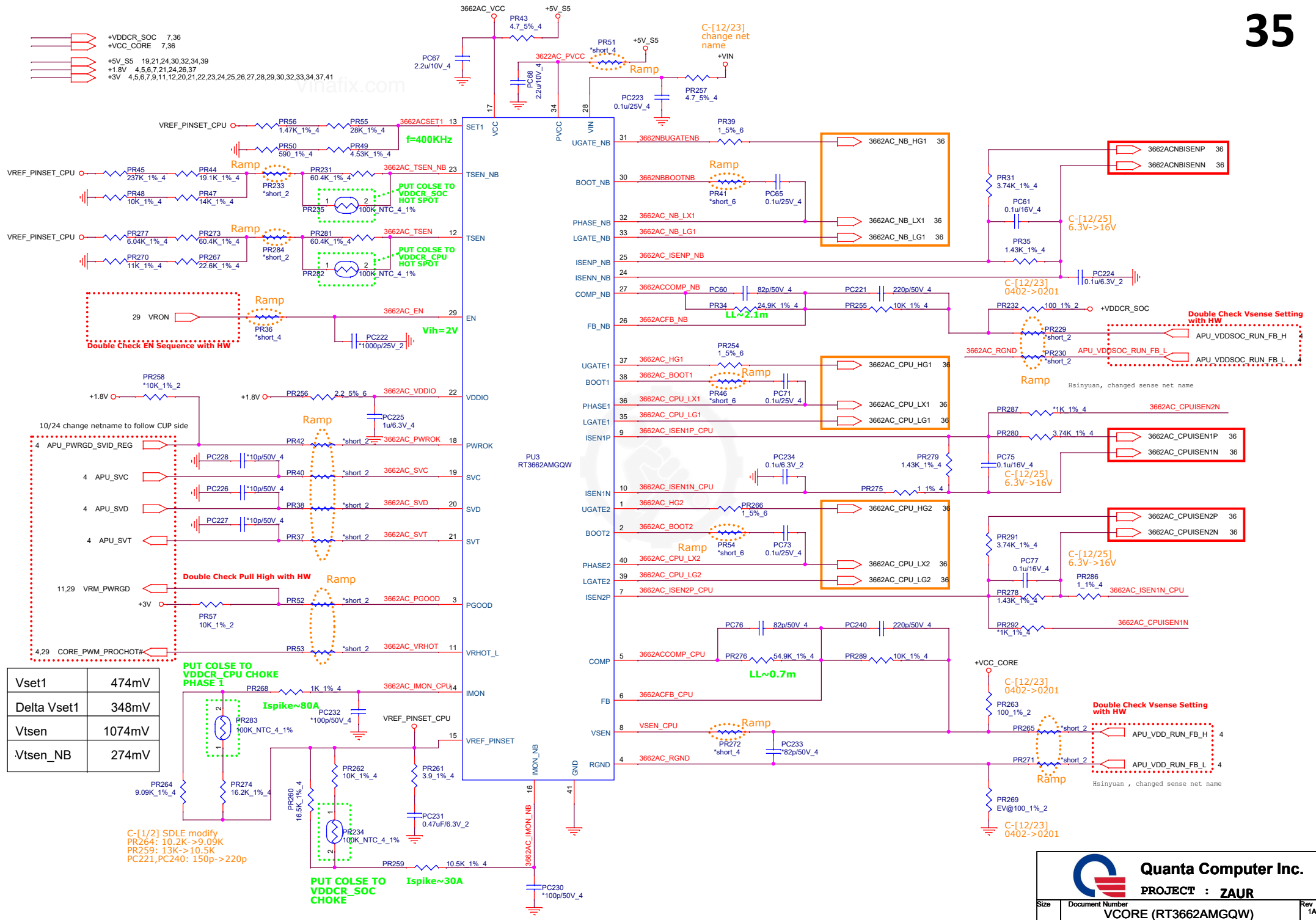
**VCC=5V**  
**(DON'T Connect to External Load)**

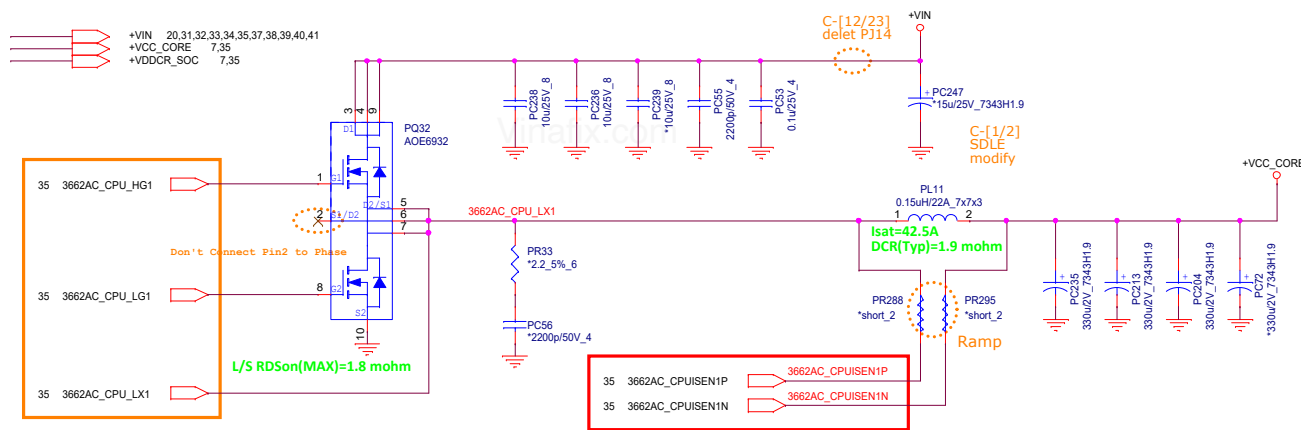





 +VIN 20,31,32,33,35,36,37,38,39,40,41  
 +1.2VSUS 3,7,9,10  
 +1.2V 22,37  
 +2.5V\_SUS 9,10  
 +VDDQ\_VTT 9,10  
 +VDDQ 9,10

	VTT_CNTL	SLP_S4	+1.2VSUS	+2.5VSUS	REF	VTT
S0	1	1	ON	ON	ON	ON
S3	0	1	ON	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF	OFF





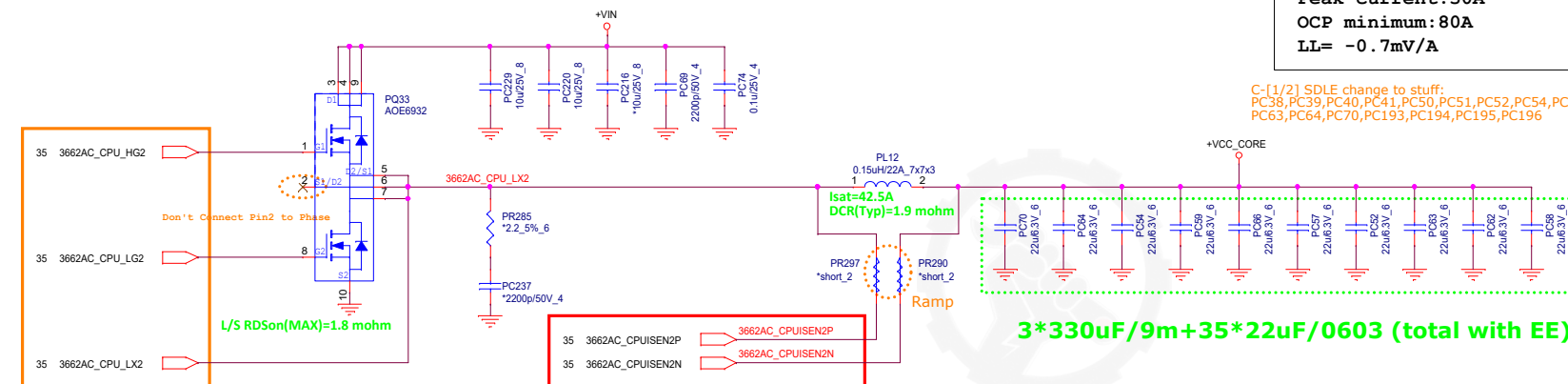
AMD Dali FP5 (15W)

```
VDDCR_VDD
Continue current:35A
Peak current:45A
OCP minimum:80A
LL= -0.7mV/A
```

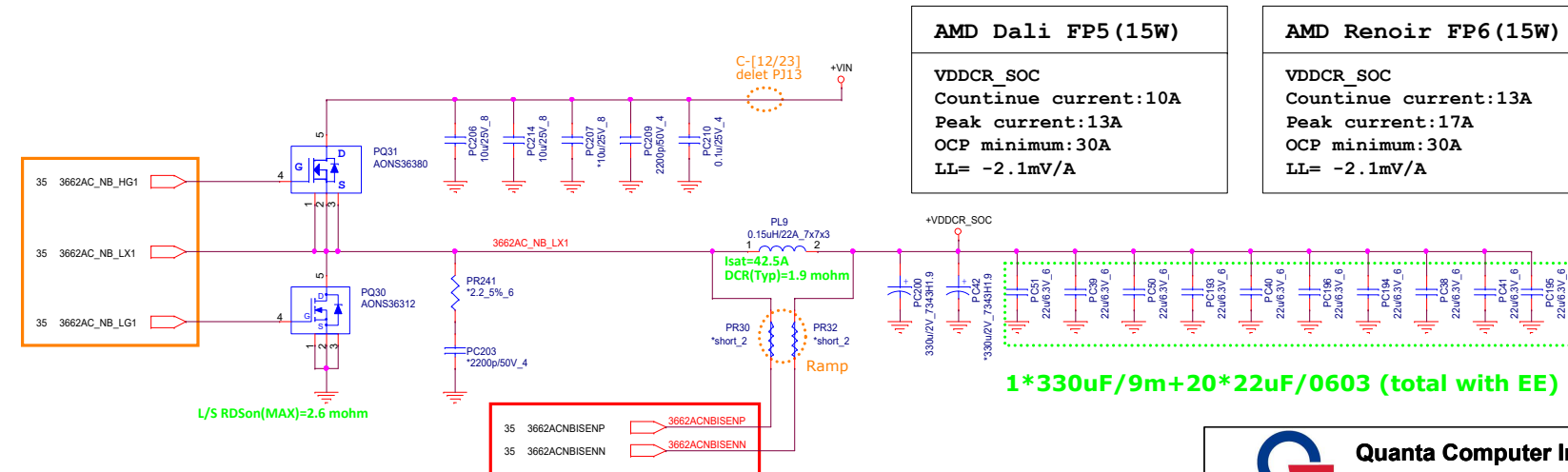
AMD Renoir FP6 (15W)

```
VDDCR_VDD
Continue current:33A
Peak current:50A
OCP minimum:80A
LL= -0.7mV/A
```

C-[1/2] SDLE change to stuff:  
PC38,PC39,PC40,PC41,PC50,PC51,PC52,PC54,PC59,  
PC63,PC64,PC70,PC193,PC194,PC195,PC196



**3\*330uF/9m+35\*22uF/0603 (total with EE)**



AMD Dali FP5 (15W)

```
VDDCR_SOC
Continue current:10A
Peak current:13A
OCP minimum:30A
LL= -2.1mV/A
```

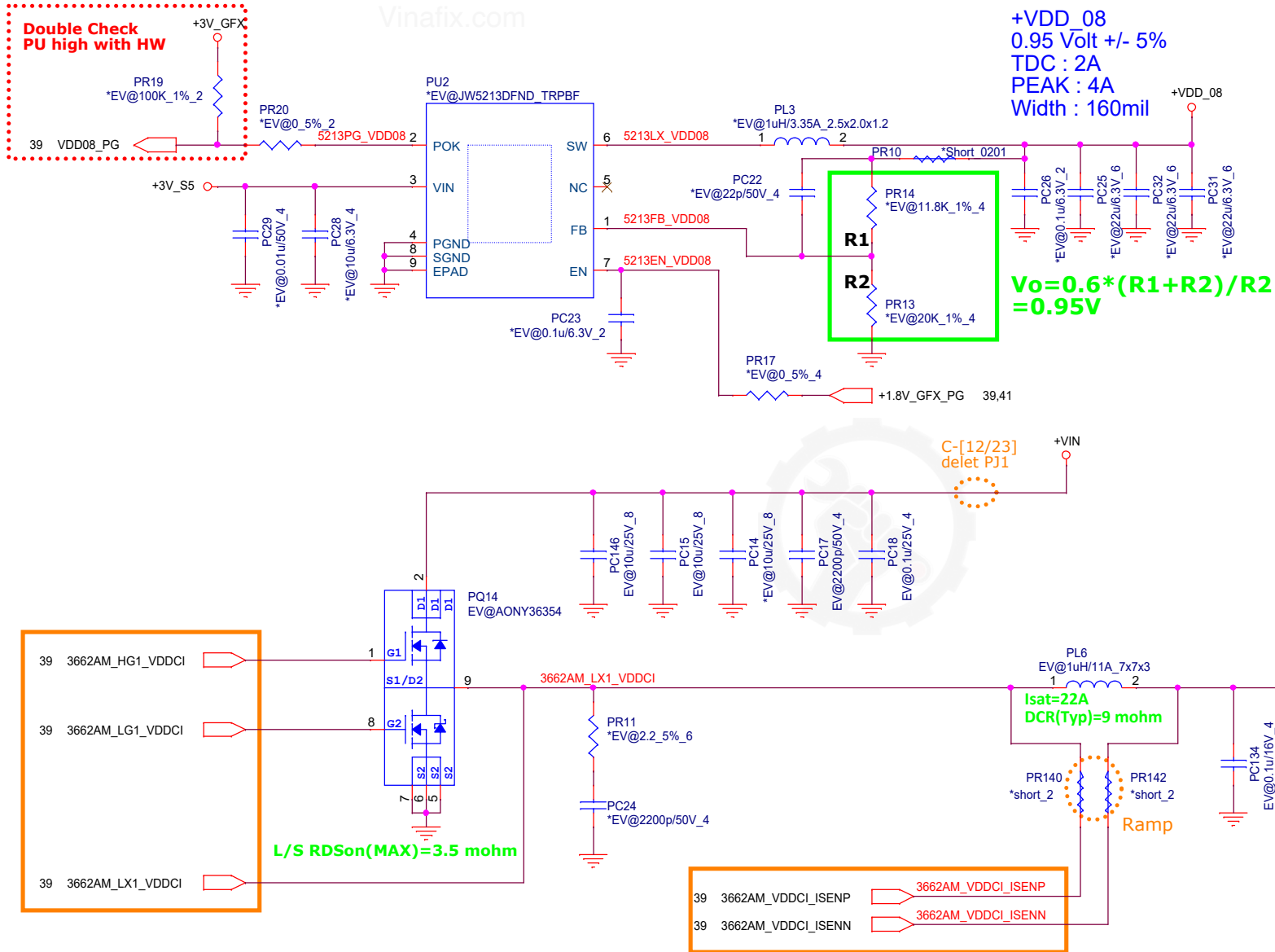
AMD Renoir FP6 (15W)

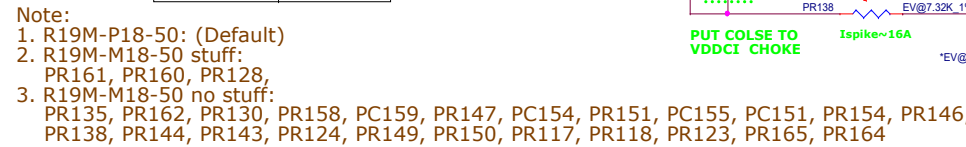
```
VDDCR_SOC
Countinue current:13A
Peak current:17A
OCP minimum:30A
LL= -2.1mV/A
```

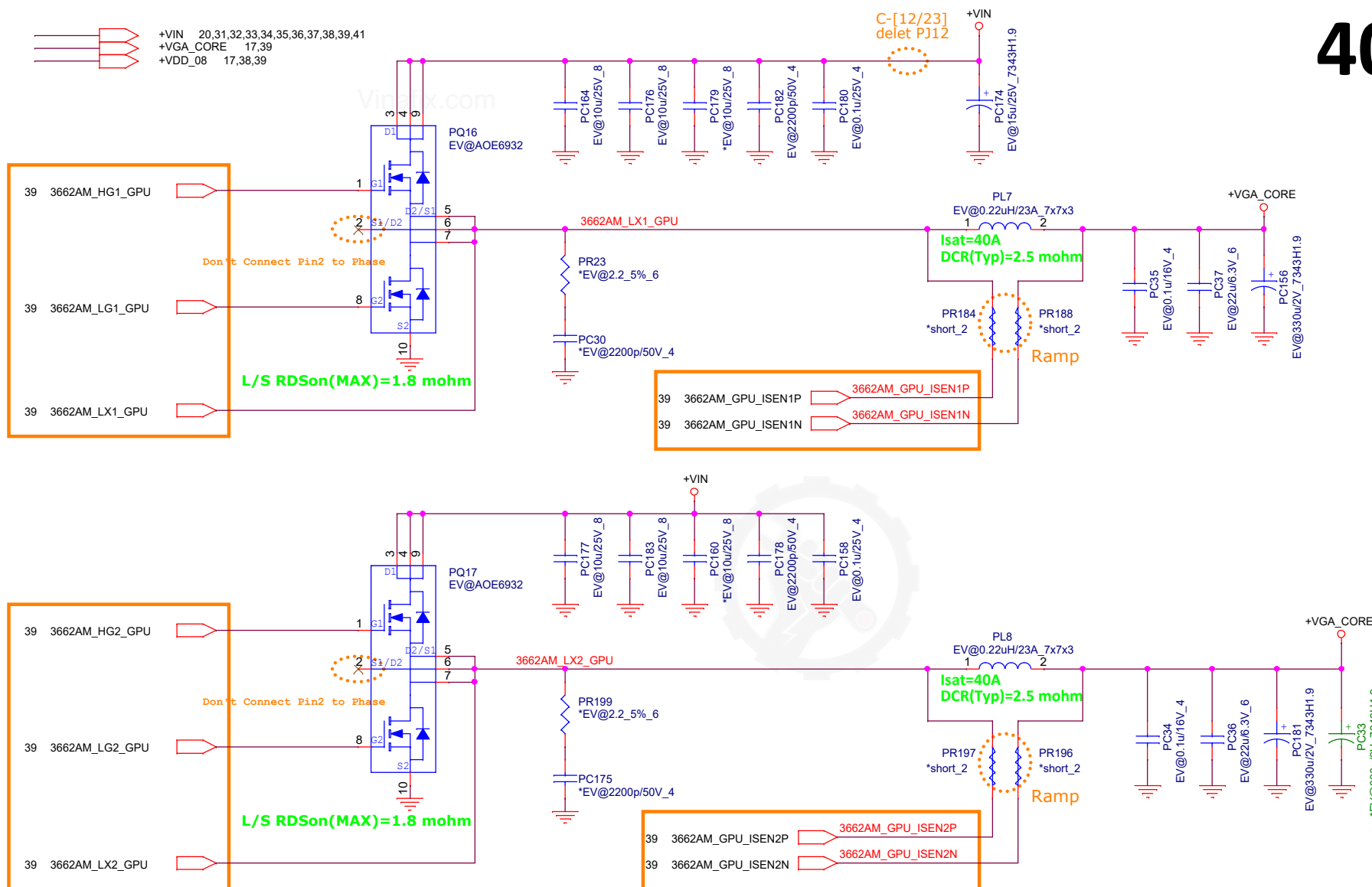
**1\*330uF/9m+20\*22uF/0603 (total with EE)**











### +VGA\_CORE(R19M-P18-50)\_18W

#### VDDC

TDC : 22A  
 EDC : 60A  
 OCP : 90A  
 LL=-0.6m

### +VGA\_CORE(R19M-M18-50)\_18W

#### VDDC + VDDCI (merged)

TDC : 18A  
 EDC : 60A  
 OCP : 90A  
 LL=-1m



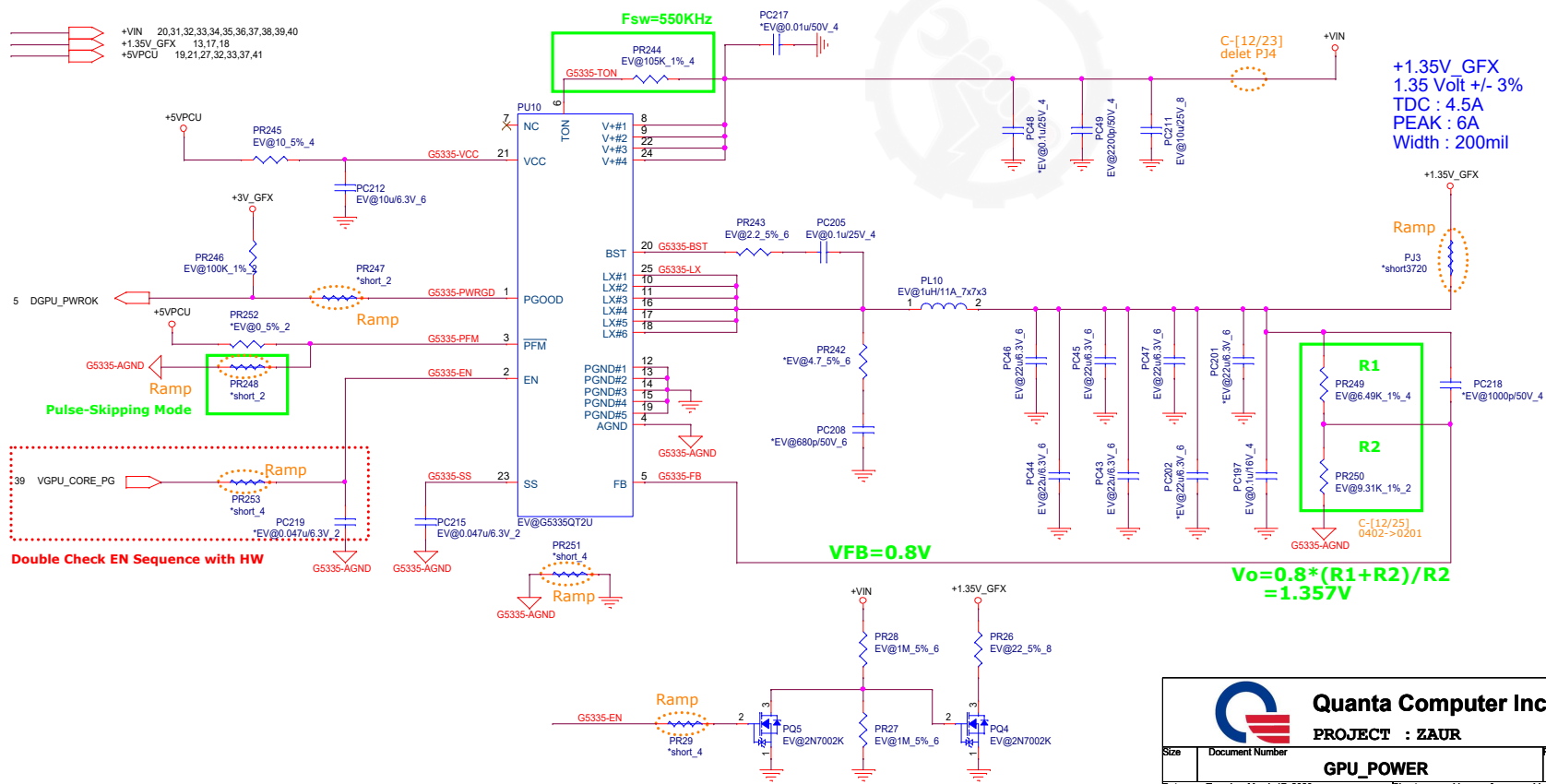
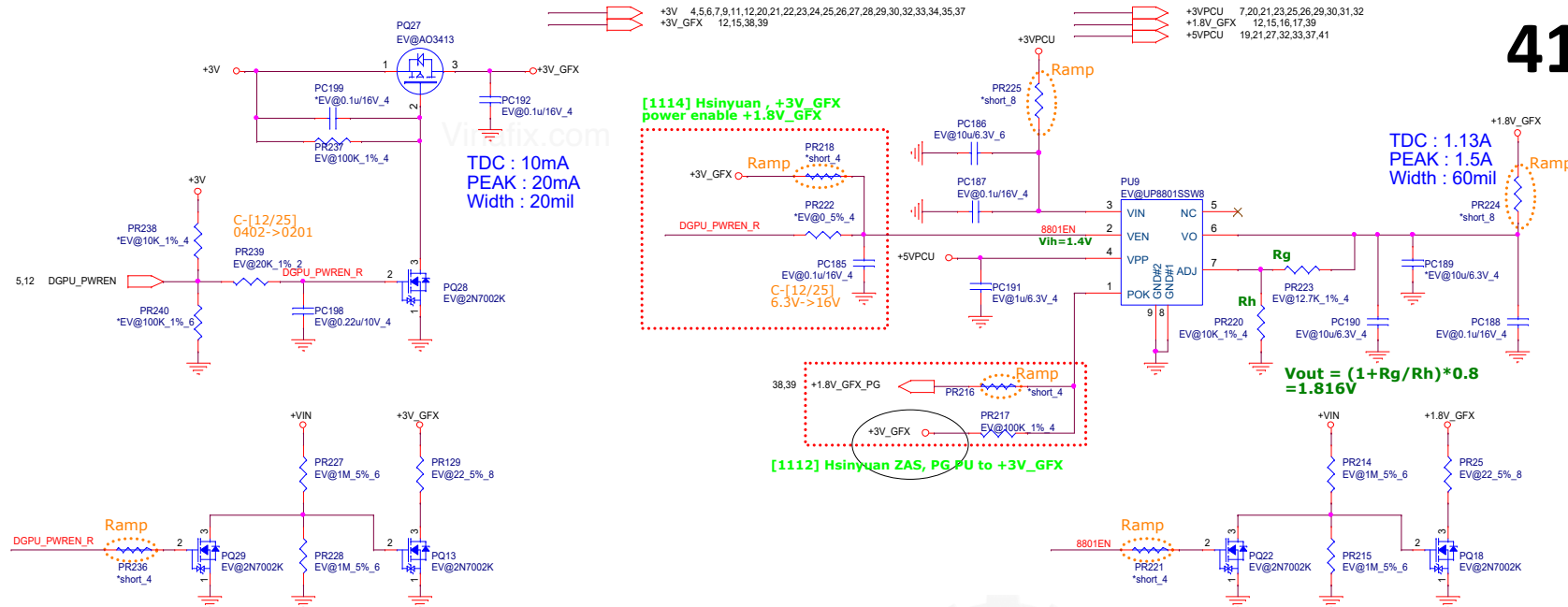
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PROJECT : ZAUR

Size Document Number  
VGAORE2 (RT3662AMGQW)

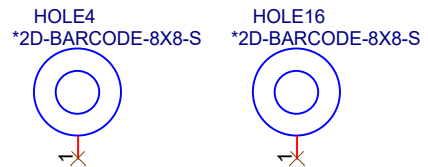
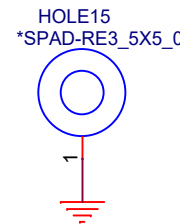
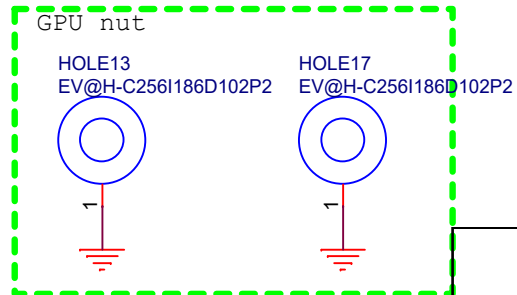
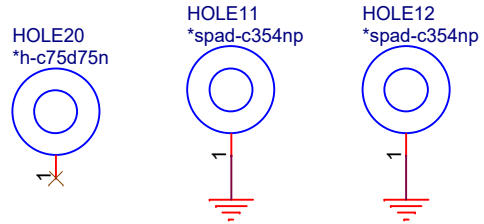
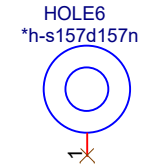
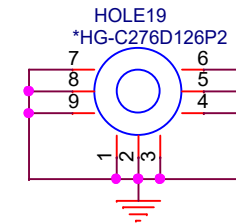
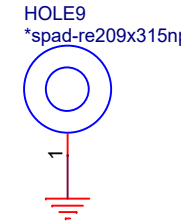
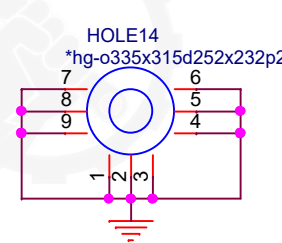
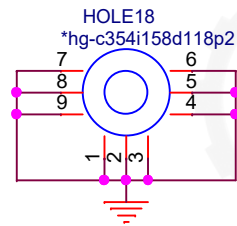
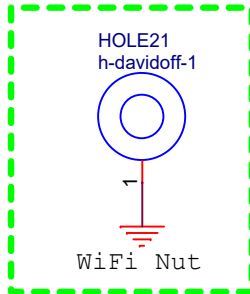
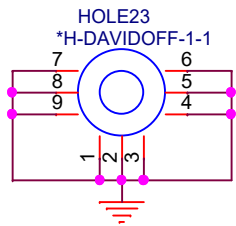
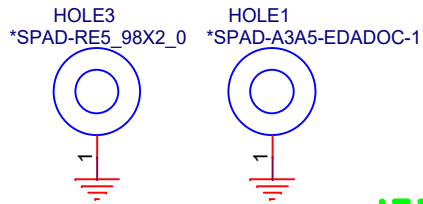
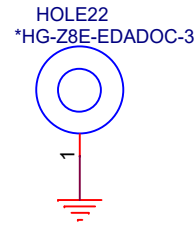
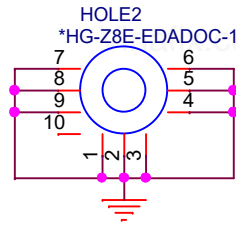
Rev  
1A

Date: Tuesday, March 17, 2020 Sheet 40 of 44



Hole

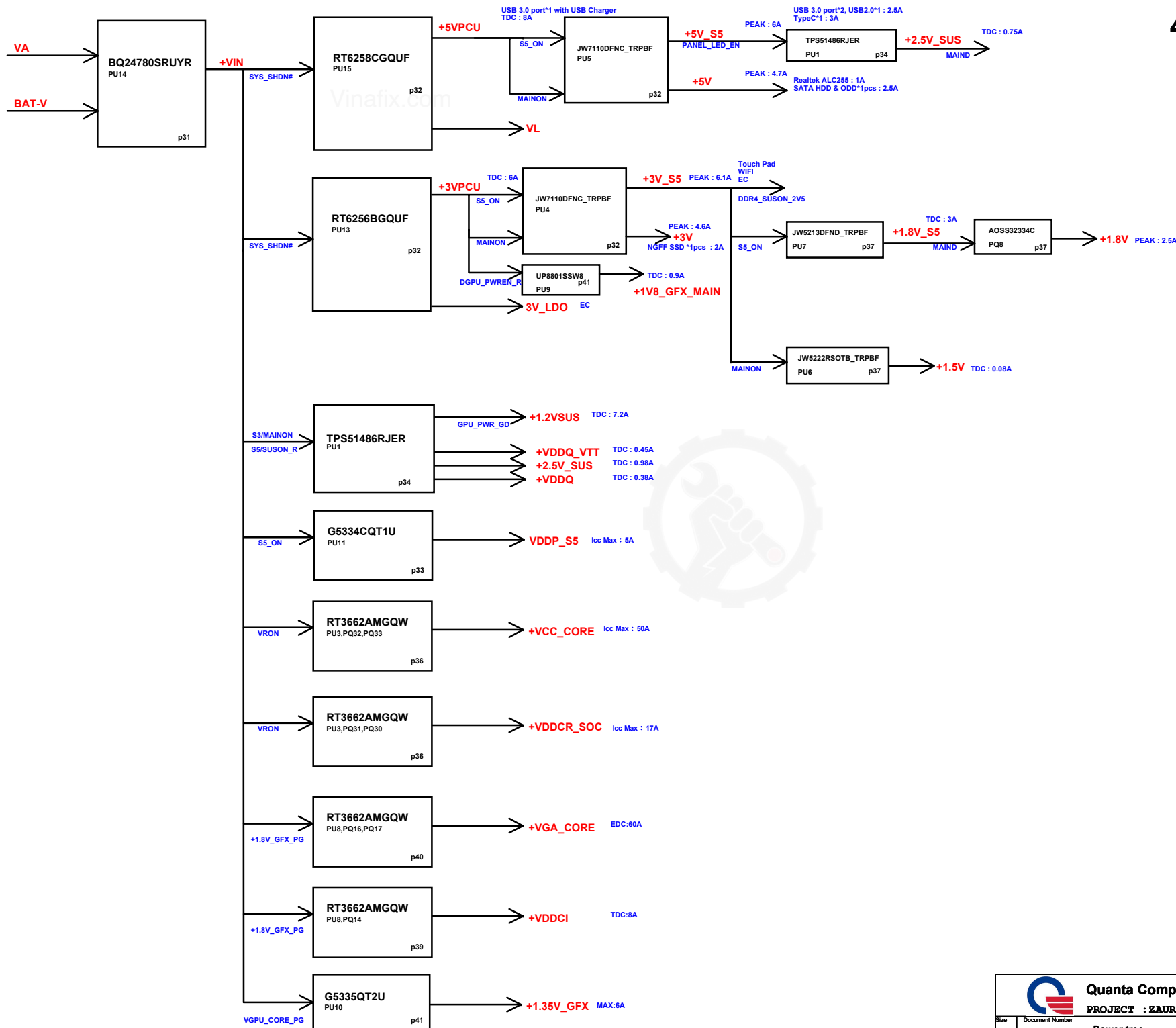
45



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PROJECT : ZAUR

Size	Document Number	Rev
	Hole	3A
Date:	Tuesday, March 17, 2020	Sheet 42 of 44





Stage	Date	CHANGE LIST
A	20191125	1. first released
C	20191217	adjust RAMID by AMD suggestion
		removed hole7
		Stuff R103 make a deault low on PEGX_RST#
		Stuff R569 4.7k and R568 4.7k for HDMI2 Eye test pass
		add SDP/DDP bom option
		APU_THERMTRIP# connect to EC new GPIO GPG0 as default, DNS SYS_SHDN# path
		change +1.8V_S5 source to +5VPCU & change +3V_S5 enable to 2ND_S5_ON for Rom sharing
		change U32 to G781-1P8 with slave address 9AH A1000781039
		reserved CCD/DMIC, TSI power gate
		change USB2 ESD protection to BC5V0F1BZ02 *2
		add +VREF_CA1 for MD
	20190317	most 0ohm modified to short pad
		R607/R608 changed to 47 ohm
		PR311 changed to 25.5K
MP		